WiPLASH

NEWSLETTER

Oct 2019-Sept 2020

Project meetings

The kickoff meeting was held on October of 2019 in Barcelona (Spain). Experts from various academic fields participate to define the future actions of the project and the guidelines to comply with the Work Packages (WPs) and the first deliverable.
Despite of the terrible affectations caused by the COVID pandemic, the following plenary meetings were held online, in accordance with the work plan. Including a project review session.

[28.05.2020] Second plenary meeting.
[24.11.2020] Third plenary meeting.
[25.11.2020] Review Session.

WiPLASH in a Nutshell

WiPLASH aims to pioneer on-chip wireless communications as a disruptive enabler towards next-generation computing systems for artificial intelligence (AI). These on-chip links must provide great scalability, reconfigurability and plasticity.
As WiPLASH is a multidisciplinary project, experts from various academic fields participate, including but not limited to material science, analog circuit design, Terahertz (THz) science, wireless communications, and computer architecture.

WiPLASH's Main Goals

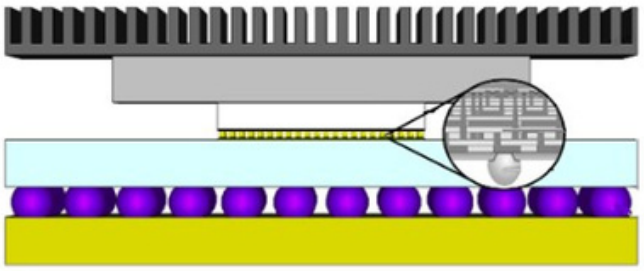
- Prototype a miniaturized and tunable graphene antenna in the terahertz band.
- Co-integrate graphene RF components with submillimeter-wave transceivers.
- Demonstrate low-power reconfigurable wireless chip-scale networks.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 863337.

WiPLASH

First Year

Throughout this year the project was quite fruitful, with 16 publications between journals and conferences. And 7 invited talks in various spaces.

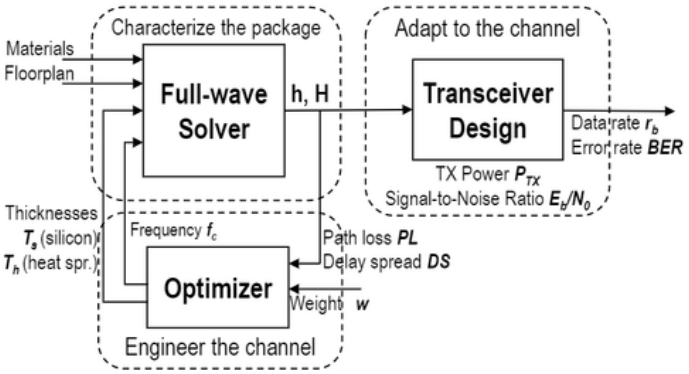


Selected Publications

Journals

- S. Abadal et al., "Wave Propagation and Channel Modeling in Chip-Scale Wireless Communications: A Survey from Millimeter-Wave to Terahertz and Optics ," IEEE Access 8, 278–293, 2019.
- **X. Timoneda et al., "Engineer the Channel and Adapt to it: Enabling Wireless Intra-Chip Communication," IEEE Transactions on Communications 68(5), 3247–3258, 2020.**
- A. Levisse et al., "Write Termination circuits for RRAM: An Holistic Approach From Technology to Application Considerations," IEEE Access 8, 109297–109308, 2020.
- W.A. Simon et al., "An in-Cache Computing Architecture for Edge Devices," IEEE Transactions on Computers, 2020.
- L. Duch et al., "Analysis of Functional Errors Produced by Long-Term Workload-Dependent BTI Degradation in Ultralow Power Processors," IEEE Transactions on Very Large Scale Integration (VLSI) Systems 28, 2122 – 2133, 2020.

The article by **Timoneda et al** proposes to take advantage of the static nature of the system and create a methodology to optimize the frequency response of the packet. This is achieved by carefully choosing the dimensions of the chip. The scenario used in the simulation is seen in the image above. The novelty of this work also lies in the modeling of the package, taking into account the influence of the material features on the channel.



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Conferences

- H. Okuhara et al., "An Energy-Efficient Low Voltage Swing Transceiver for mW-Range IoT End-Nodes," in Proc. IEEE International Symposium on Circuits and Systems (ISCAS), Sevilla, Spain, pp. 1-5, 2020.
- G. Ottavi et al., "Mixed-Precision RISC-V Processor for Extreme-Edge DNN Inference," in Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Limassol, Cyprus, pp. 512-517, 2020.
- A. Levisse et al., "Exploration Methodology for BTI-Induced Failures on RRAM-Based Edge AI Systems," in Proc. IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), Barcelona, Spain, 2020, pp. 1549–1552.
- **H. Najibi et al., "Enabling Optimal Power Generation of Flow Cell Arrays in 3D MPSoC with On-Chip Switched Capacitor Converters," in Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Limassol, Cyprus, 2020. (Best Paper Award)**
- R. Guirado et al., "Understanding the Impact of On-Chip Communication on DNN Accelerator Performance," in Proc. ICECS '19, Genova, Italy, November 2019.

Best Paper Award

[2020] The project members Alexandre Lévisse, Marina Zapater and David Atienza received a best paper award at ISVLSI2020. H. Najibi et al., "Enabling Optimal Power Generation of Flow Cell Arrays in 3D MPSoC with On-Chip Switched Capacitor Converters," in Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Limassol, Cyprus.
In this paper they assess the power generation performance of Flow Cell Arrays (FCAs) by means of high efficiency and low area Switched Capacitor converters.

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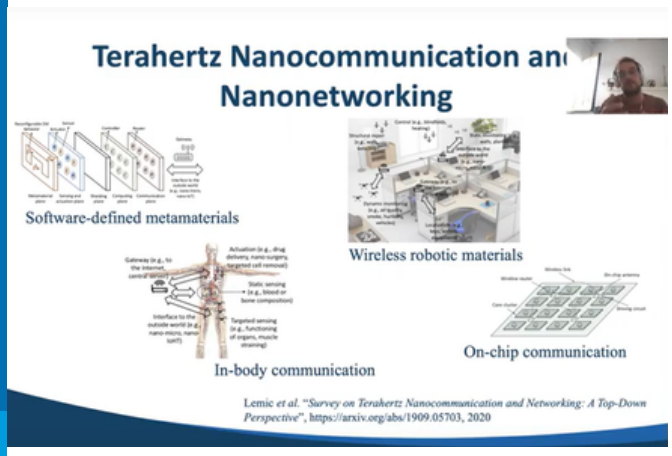
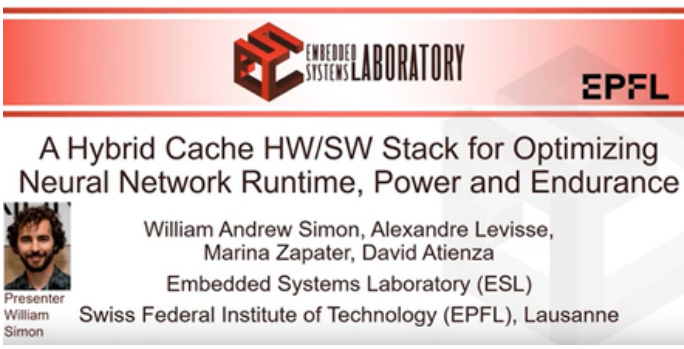
Invited Talks

- Z. Wang, "Wafer Scale Integration of Graphene – Progress and Outlook," Graphene 2020 Online Conference, Oct. 2020.
- Z. Wang, "Metal-Insulator-Graphene RF Diodes: From Devices to Integrated Circuits," Joint Spring MOS-AK Workshop and Symposium on Schottky Barrier MOS (SB-MOS) devices with IEEE EDS Mini-Colloquium on „Non-conventional Devices and Technologies", October 2020.
- A. Sebastian et al., "Unconventional computing and what it means for the future of interconnects," International Workshop on Network on Chip Architectures (NoCArc), held within the IEEE/ACM International Symposium on Microarchitecture, October 2020.
- S. Abadal and F. Lemic, "Terahertz Nanocommunication and Networking: Emerging Applications, Approaches, and Open Challenges," ACM International Conference on Nanoscale Computing and Communication (NANOCOM), September 2020.
- A. Levisse et al., "Demonstrating In-Cache Computing Thanks to Cross-Layer Design Methodologies," Design Automation and Test in Europe (DATE), Special Session on In-Memory Computing for Edge AI, Grenoble (FR), Virtual Event April 2020.



Dr. Sergi Abadal and Dr. Filip Lemic present their views on the progress, possibilities and pending questions of nanotechnology in the THz band at the ACM International Conference on Nanoscale Computing and Communication (NanoCom), 2020. **Link**

Presentation of the published paper of the same name. SHyCache is introduced: a Stack for Hybrid Caches that enables deterministic data placement in hybrid caches. **Link**



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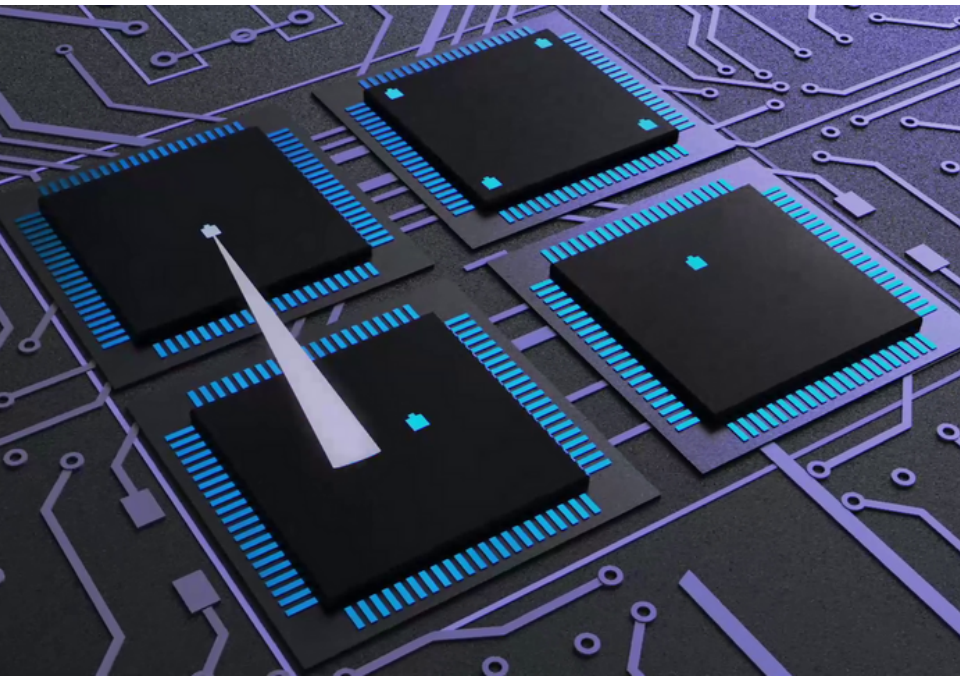
News and Press Coverage

[1.10.2019] AMO blog: AMO Launches Three New FET Open Projects**. Link**

[1.10.2019] Press release RWTH Aachen: EU to Fund Three Groundbreaking Research Ideas. **Link**.

[7-11.11.2019] WiPLASH at IEDM: WiPLASH partners met at IEEE International Electron Devices Meeting in San Francisco.

Comunication and outreach



The WiPLASH consortium released a video explaining the essence of the research. The objective of the project to solve the problem of the interconnection between nanotechnology and wireless communications within a computer chip is addressed. If successful, WiPLASH will lay the foundation for a new generation of processors with the performance of specialized accelerators but without loss of generality.
Link

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First Year

WiPLASH's Consortium

Final Remarks

The session held on November 25 was attended by three reviewers who were overall satisfied with the project status and feedback related to scientific progress. **This meeting officially concluded the first year of WiPLASH**.

In the Review Session every WP responsible gave a brief presentation of their advences, objectives, developed work, future actions and some expected results. These briefings were followed by a Q&A session. **The first year of WiPLASH was finished with flying colors.**

www.wiplash.eu

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