Horizon 2020 Program (2014-2020)

FET-Open Novel ideas for radically new technologies

FETOPEN-01-2018-2019-2020

Architecting More than Moore – Wireless Plasticity for Massive Heterogeneous Computer Architectures †

D2.3: Full transceiver/antenna subsystem with high performance ready for measurements

Contractual Date of Delivery	30/09/2023
Actual Date of Delivery	13/10/2023
Deliverable Security Class	Public
Editor	Renato Negra, Zhenxing Wang
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† This project is supported by the European Commission under the Horizon 2020 Program with Grant agreement no: 863337

Document Revisions & Quality Assurance

Deliverable Number	D2.3
Deliverable Responsible	AMO
Work Package	WP2
Main Editor	Renato Negra, Zhenxing Wang

Internal Reviewers

1. Muh-Dey Wei (RWTH)
2. Sergi Abadal (UPC)

Revisions

Version	Date	By	Overview
1.0	13/10/2023	Zhenxing Wang	Final version for submission
0.2	12/10/2023	Muh-Dey Wei, Sergi Abadal	Version modified after review
0.1	29/9/2023	Renato Negra, Zhenxing Wang	First draft

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Executive Summary

Currently, there are challenges in advancing RF systems based on 2D materials. Although graphene possesses high mobility and conductivity, its lack of an energy bandgap inherently limits its performance in transistors. Nonetheless, graphene-based diodes exhibit exceptional behaviour in high-frequency applications and have been used in this project to design MMIC circuits and subsystems in the collaboration between AMO and RWTH. Notably, this work achieves the combination of two distinct CVD 2D material-based devices on a single chip: graphene-based diodes and MoS_2 FETs, as well as the integration of antennae and graphene-based circuits.

A combination of a metal antenna array with graphene-based phase shifters was studied in order to demonstrate both the cointegration capability as well as to explore the feasibility of steerable antenna arrays in the available technology. Although the designed and fabricated circuits show good performance in simulations, the measured characteristics of the phase shifters falls behind the expectations. In order to improve the performance, a more stable connection between the developed MIG-device model and the current version of the MMIC process has to be established. Nevertheless, the realisation of a steerable antenna array could be demonstrated.

Different approaches have been studied for implementing both transmitters and receiver frontend using graphene devices. In this project we have successfully demonstrated the design of parametric up- and down-converters with very little DC power consumption and low footprint. The parametric concept has been demonstrated by using a commercial SiGe process with very good results in measurements. The developed concept is very well suited to be applied to graphene-based technologies as was demonstrated previously in the frame of this project. The realised frontend circuits show substantial conversion gain although the transistors are used in a diode-configuration, thus demonstrating the feasibility of the proposed concepts to be applied to the graphene technology. The concept has been successfully demonstrated for both transmitter and receiver frontends.

Further frontend concepts have been explored within WiPLASH. For the transmitter side, a mixerless approach has been studied and realised in the MMIC process. Simulation results of different architectures have been investigated and compared with each other. Due to the limitations of the MIG diodes and the process, the concepts have been designed at a lower frequency of 2.4 GHz in order to assess the advantages and disadvantages of the concepts. Nevertheless, a study on the scalability of the approaches shows that using transmission lines, the mixerless transmitter can be also implemented at higher frequencies. The designed circuits are in the process of fabrication and hence no measurement results will be available in the frame of this project.

In summary, the work carried out shows that it is possible to realise high frequency circuits based on graphene devices by adapting the circuit topologies to the available devices and by exploiting the unique properties. Moreover, these circuits can be combined with graphene antennae, but this requires some further process development.

Abbreviations and Acronyms

NoC	Network-on-Chip
MMIC	Monolithic Microwave Integrated Circuits
MIG	Metal-insulator-graphene
RF	Radio frequency
QAM	Quadrature amplitude modulation
LO	Local oscillator
GFET	Graphene field-effect transistor
DC	Direct current
Tx	Transmitter
Rx	Receiver
SiGe	Silicon Germanium
HBT	Heterojunction bipolar transistor
PAMP	Parametric amplification
PDC	Parametric down-conversion
PUC	Parametric up-conversion
BW	Bandwidth
PIFA	Planar inverted-F antenna
IF	Intermediate frequency
USB	Upper sideband
LSB	Lower sideband
BEOL	Back-end-of-line
OFDM	Orthogonal frequency-division multiplexing
DAC	Digital-to-analogue converter
PI	Polyimide
BLC	Branch-line coupler
EM	Electromagnetic
EVM	Error vector magnitude
TMDC	Transition metal dichalcogenides
CVD	Chemical vapor deposition
TRF	Thin-film resistors
MIM	Metal-insulator-metal
RL	Return loss

The *WiPLASH* consortium is composed by:

UPC	Coordinator	Spain
IBM	Beneficiary	Switzerland
UNIBO	Beneficiary	Italy
EPFL	Beneficiary	Switzerland
AMO	Beneficiary	Germany
UoS	Beneficiary	Germany
RWTH	Beneficiary	Germany

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1 Introduction

Graphene is a promising candidate among the numerous 2D materials for high frequency devices due to its outstanding electrical and mechanical properties. As an emerging thin-film technology that fulfils the requirements for high frequency applications, together with the flexibility due to its 2D nature make graphene a perfect choice for RF, millimetre, and submillimetre-wave circuit applications both on rigid and flexible substrates. However, due to the gapless band structure of graphene, the reported DC transfer characteristics of state-of-the-art graphene field-effect-transistors (GFETs) show no widely useful current saturation. Hence, the transistor intrinsic DC gain (A_v) is low, and the large drain-source conductance (g_{DS}) leads to maximum frequencies of oscillation (f_{max}) behind the expectations. Consequently, the reported graphene receivers based on the use of GFETs transfer transconductance (g_m) are limited in the operating frequency and provide low conversion gain (CG).

An alternative way to amplify an electric signal is the parametric amplification (PAMP) concept, which relies on varying the reactance of an inductance or capacitance other than varying the transconductance in the traditional transistor implementation. In this project we have presented the utilisation of the quantum capacitance of graphene in a distinct PDC to achieve positive CG avoiding the GFETs limitations in the conventional transconductance amplification scheme. As soon as the graphene technology becomes stable enough for high frequency design, this concept which was validated in a SiGe technology will be able to open new applications and thus, markets for graphene-based high-frequency electronics.

This deliverable reports the progress made within the WiPLASH project in terms of the cointegration of antennae and graphene-based high frequency circuits and describes the achievements. First, the details about the design of metal antennae and the integration with graphene-based circuits is detailed in Section 2. Successively, different approaches for designing transmitter circuits for wireless chip-to-chip communication applications based on the available graphene device based MMIC process are assessed in Sections 3 and 4. Because the MMIC process provides diodes which perform well at microwave and millimetre-wave frequencies, both parametric concepts for both amplification and frequency conversion have been studied. The circuits have been fabricated in a commercial semiconductor technology to validate the concepts. However, the developed concepts are actually tailored to the device characteristics of the graphene diode, so that they can be ported to a mature and stable graphene-based MMIC technology. Besides the parametric approaches, different mixerless transmitters have been designed based on graphene diodes. All of these circuits can be cointegrated with both metal antennae with the described MMIC process in Section 5. Moreover, other TMDCs devices can be included in this fabrication process as successfully demonstrated in this project. Thus, the project has demonstrated that as soon as the graphene-based antennae developed within WiPLASH will be operating in a frequency range in which circuits based on the available graphene diodes can be successfully designed, a cointegration of both is possible and will provide a flexible platform for the integration of chip-to-chip wireless communication frontends with a high degree of plasticity.

2 Metal antenna and phase shifter design

One step on the line of a full cointegration of graphene-based circuits and antennae is the successful design and manufacturing of graphene-based integrated circuits at millimetre-wave frequencies. Based on the requirements of the project where chip-to-chip wireless communication is explored, it has been found that the capability of steering to some extent spatially the data transmission is advantageous in terms of power consumption and data throughput. Based on these results, an antenna array with beam steering capabilities was designed using phase-shifters to control the phase of the signals at each antenna element of the array. Because of fabrication issues in producing nanoscale graphene-devices, the proof-of-concept circuits have been designed for the millimetre frequency range, in which the devices with the available feature sizes could operate well. The tuneable antenna array mimics thus the tuneable graphene-based antenna. Although the advantages of graphene antennas are extreme miniaturization and mechanical flexibility, they can only be implemented at THz-frequencies due to the limited mobility of transferred graphene sheets. However, at these frequencies, the available graphene devices would not perform well.

Numerous planar integrated antenna configurations have been designed as shown in Figure 1. Their far-field simulations are compared to understand the effects of different substrate thicknesses and materials on which graphene-based devices can be implemented. A low dielectric constant provides higher radiation efficiency yet it causes larger patches. According to simulations, the rectangular on-chip patch antenna gives the best gain performance but suffers from a narrow bandwidth (BW). The BW can be increased by employing an E-shape patch. Although the bandwidth can be increased by this technique the radiation efficiency is compromised. The simulation results on quartz are plotted in Figure 2, Figure 3, and Figure 4. Three different antennae have been fabricated simultaneously on three different substrate technologies as shown in Figure 5 and they are characterized as plotted in Figure 6. Most of the antennae exhibit similar matching performances in the EM simulation results. Near- and far-field measurements have not been performed yet due to the required setup. On one hand the fragile metallisation pads can be easily probed with probe tips, however, in this frequency range the wafer prober environment is a severe limitation for meaningful data. Bonding the chips on a carrier board to connect the circuit was tried, but unfortunately delamination of the probe pads was observed during bonding, so that the measurements could not yet be performed.

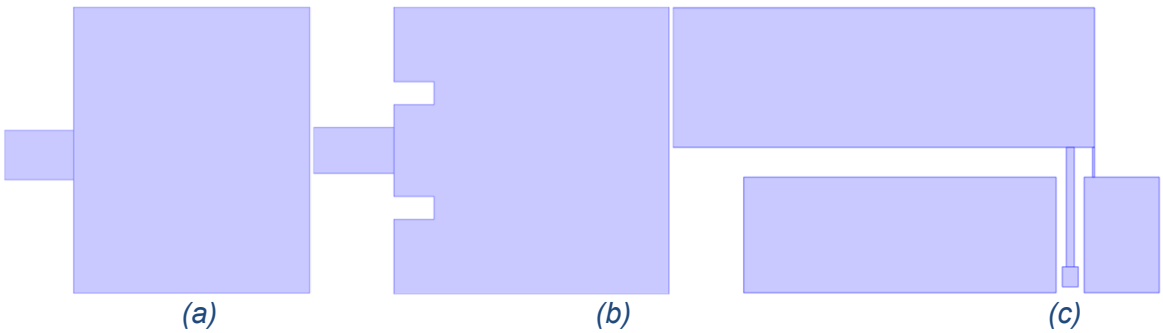


Figure 1 Various patch antenna designs: a) rectangular, b) E-shape, and c) planar inverted F antenna

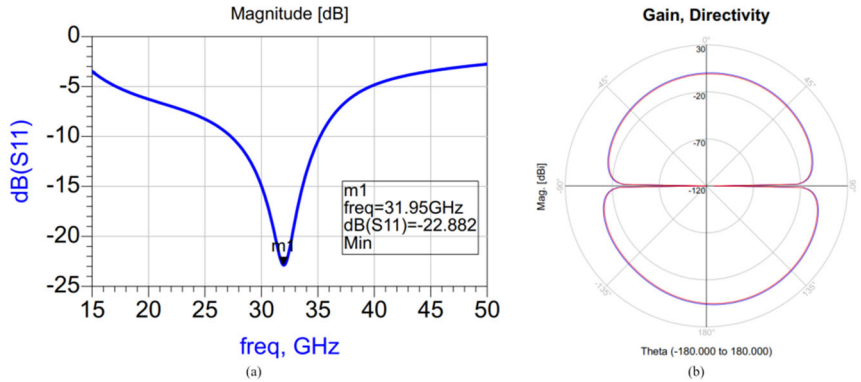


Figure 2 Simulation results of the designed rectangular patch antenna on quartz: a) EM simulation indicating RL and b) the simulated far-field radiation pattern

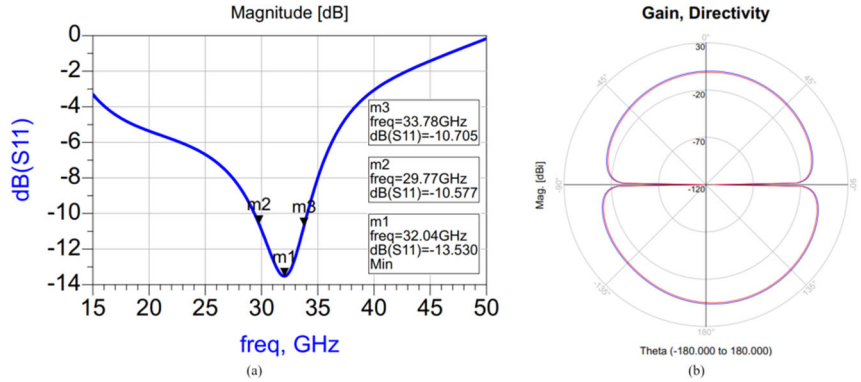


Figure 3 Simulation results of designed and manufactured E-shape patch antenna on quartz substrate: a) EM simulation indicating matching performance and b) simulated far-field radiation pattern

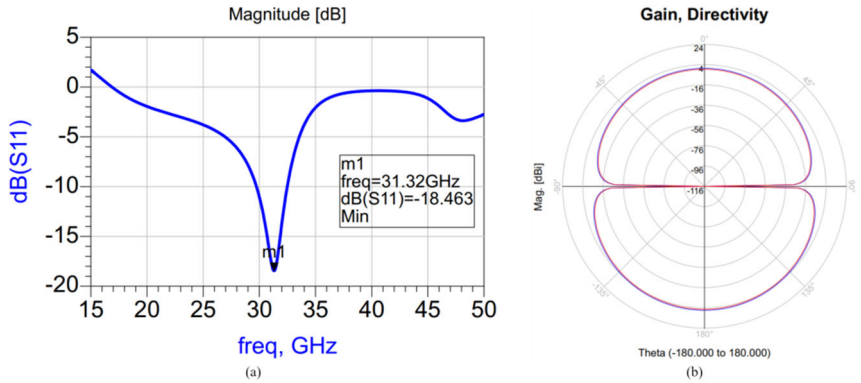


Figure 4 Simulation results of the PIFA on quartz substrate: a) EM simulation indicating matching performance and b) the simulated far-field radiation pattern

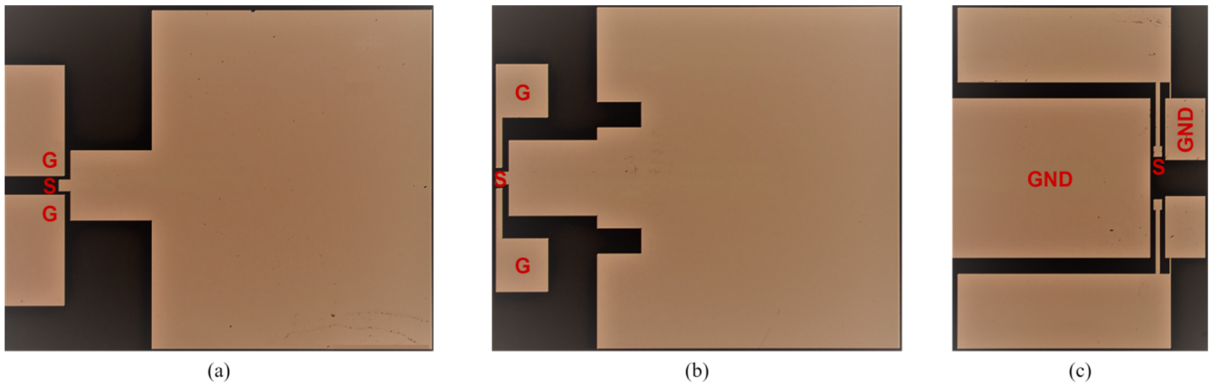


Figure 5 Chip micrograph of the fabricated patch antennas on quartz substrate: a) rectangular, b) E-shape, and c) PIFA antennae

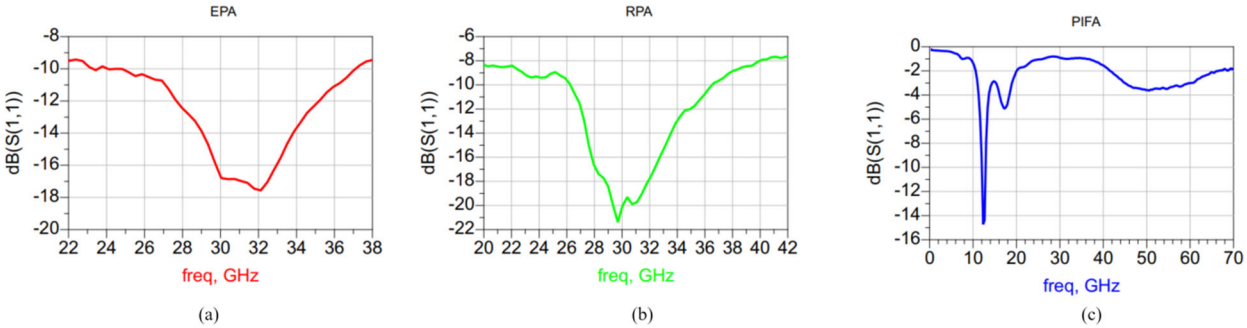


Figure 6 Measured S_{11} of the fabricated patch antennae on quartz substrate: a) E shape, b) rectangular, and c) PIFA designed for operation at 10 GHz

2.1 Phase shifter

In order to control the antenna beam, integrated phase shifters based on graphene devices are necessary. The designed MMIC phase shifter comprises three MIG diodes in a T-shape configuration, as shown in Figure 7. Besides the MIG diodes, the circuit also comprises a bias resistance (R_{bias}) and a shunt inductor (L_{shunt}). The diode impedance together with the shunt inductance L_{shunt} mainly form the resonance branch of the high frequency matching. R_{bias} serves as RF block resistor to provide an RF open circuit at the DC branch. The value of R_{bias} affects critically the insertion loss (IL) of the phase shifter.

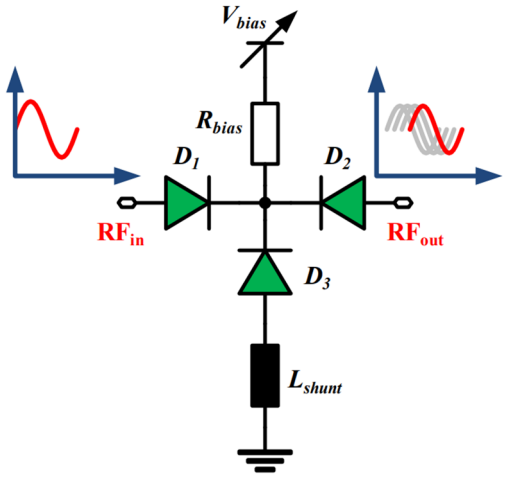


Figure 7 Conceptual block diagram of the designed T-shape phase shifter exploiting three graphene diodes

The initial design has relied on off-chip R_{bias} in order to be able to compensate the fabrication tolerances of the graphene MMIC process. After fabrication of the designs shown in Figure 8, it was observed that the IL performance is worse than expected and could also not be improved considerably by tuning the resistor. The poor IL characteristic is thought to originate from the unwanted transmission loss of the RF signal trough the bias branch. The fabricated prototype occupies less than 0.42 mm^2 of chip area including contact pads. The phase shifter is designed to operate over a bandwidth of 10 GHz at a centre frequency of 30 GHz.

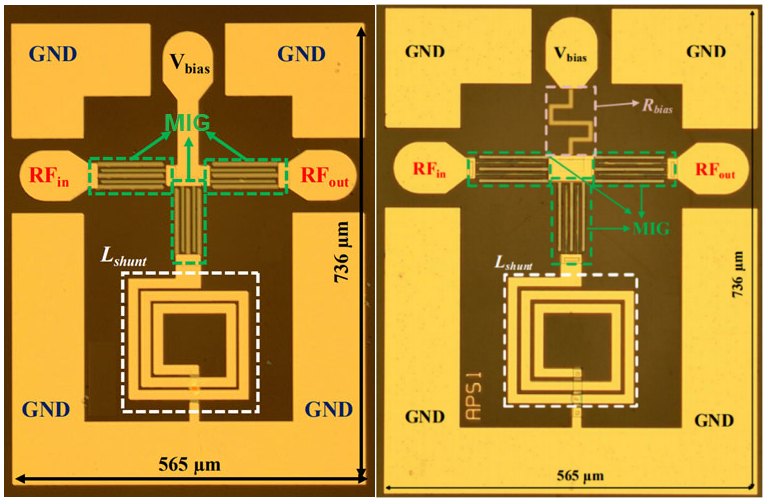


Figure 8 T-shape phase shifter chip micrographs: a) Former design without bias resistance and b) Updated version including 2 kΩ resistance layer

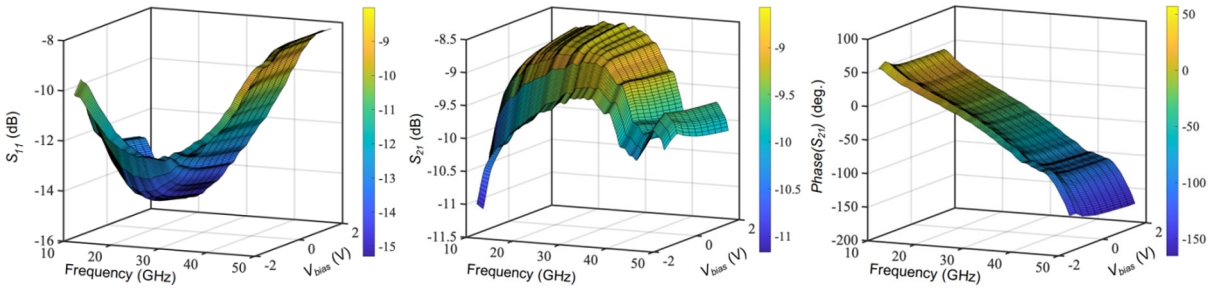


Figure 9 Measurement results of phase shifter: a) S11(dB), b) S21(dB) and c) S21(phase)

The measurement has been performed at different bias voltages from -1.5 V to 1.5 V. Figure 9 shows the measured return loss of the T-shape phase shifter, which demonstrate that the fabricated phase shifter exhibits an S_{11} better than -14 dB for the frequency range from 25–35 GHz. The measured magnitude of S_{21} is plotted in Figure 9. The magnitude in the desired frequency band is -9.1 dB with ± 0.6 dB of tolerance. The maximum tuneable phase difference is measured as 24° at 30 GHz.

2.1.1 Reflective-type phase shifters

Because of the low phase tuning range of the T-shaped phase shifter, other architectures have been investigated such as a reflective-type phase shifter as shown in Figure 10 and Figure 11. A two-stage reflective type phase shifter was designed to reduce the insertion loss as well as to increase the phase tuning range of a single-stage phase shifter. The simulated results are plotted in Figure 12 and show great performance in terms of return loss, insertion loss, and tuneable phase range. Whereas S_{11} is better than -20 dB, simulated S_{21} is -2.3 dB with a tolerance of ± 0.5 dB. The phase shifting capability of this configuration at 30 GHz is simulated as 120° using the developed MIG diode model. The area of the chip is less than 0.92 mm^2.

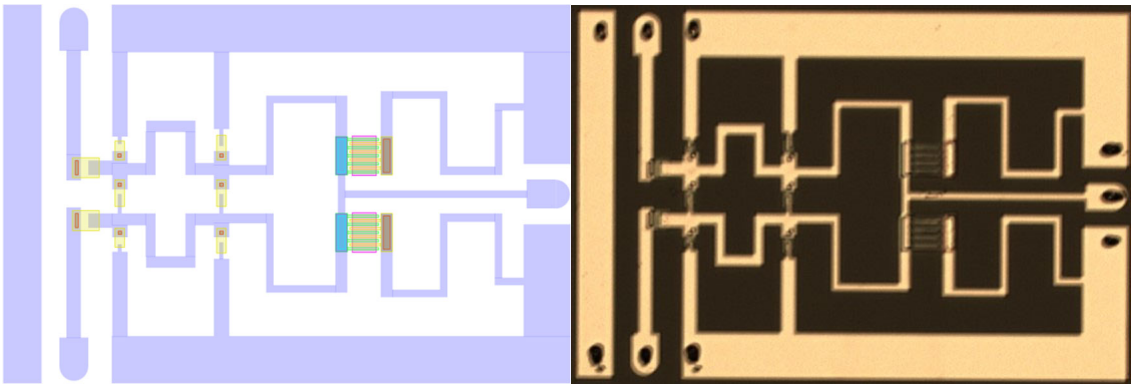


Figure 10 Layout and chip micrograph of the single-stage RTPS consisting of two 5x50 µm MIG diodes

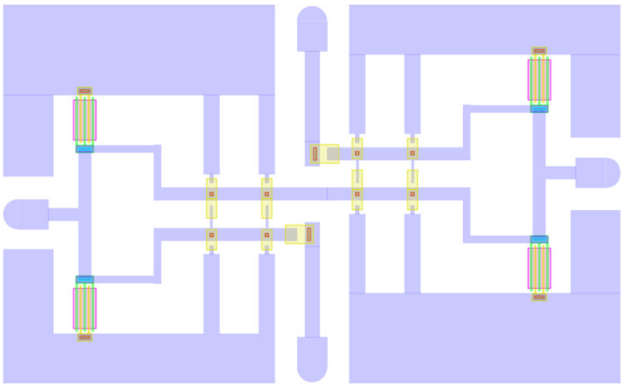
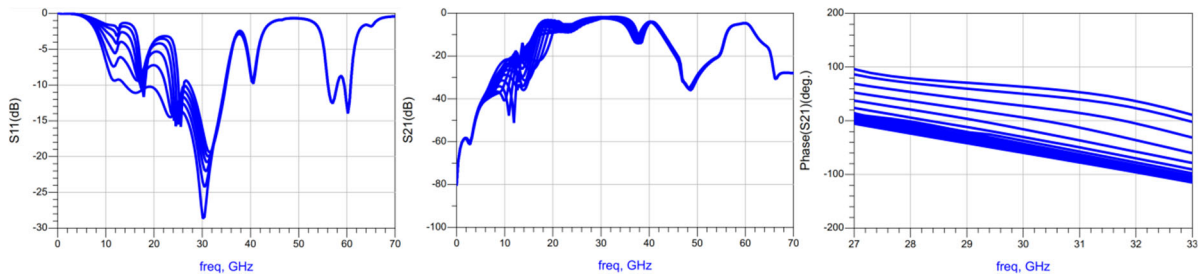


Figure 11: Layout of the two-stage RTPS consisting of four 3x80 µm MIG diodes



a) b) c)

Figure 12 Simulation results of the two-stage RTPS: a) S_{11}(dB), b) S_{21}(dB), and c) S_{21}(phase)

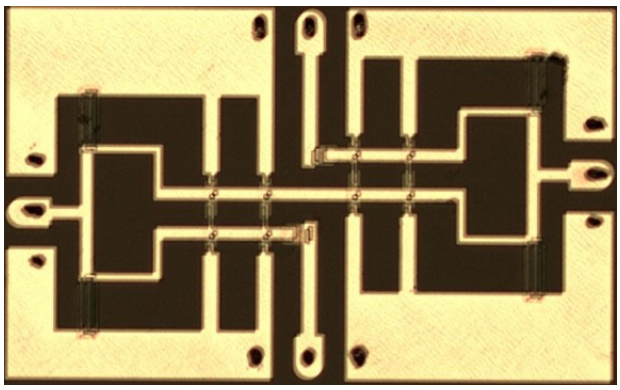


Figure 13 Chip micrograph of the two-stage RTPS

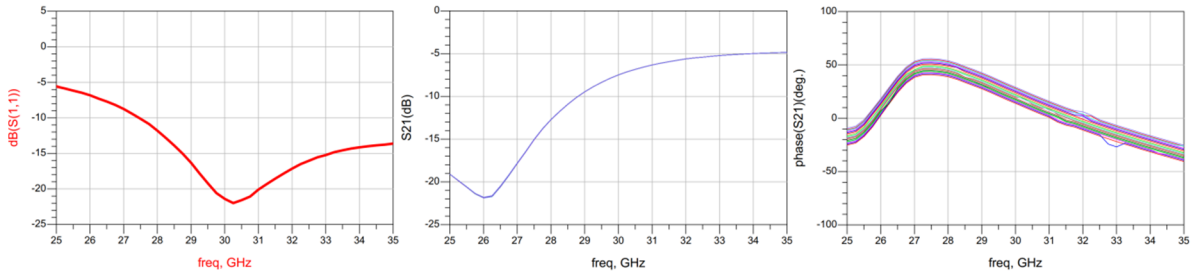


Figure 14 Measurement data of the two-stage RTPS: a) S_{11}(dB), b) S_{21}(dB), and c) S_{21}(phase)

The measurements have been performed at different bias voltages from -2 V to 2 V. Figure 14 shows the return loss of two stage RTPS. It can be seen that the prototype exhibits an S_{11} better than -15 dB in the frequency band from 28–32 GHz. The measured magnitude of S_{21} is also provided in Figure 14. The magnitude in the design range is -7.4 dB with ± 0.4 dB of variation. The maximum phase tuning range was measured to be only 15° at 30 GHz compared to the simulated 120°.

3 Parametric amplifiers (PAMP) and frequency converters

Parametric amplifiers (PAMP) and frequency converters were extensively studied in the 1950s and 1960s [1]-[8]. Rather than varying a transconductance, as in the now traditional transistor implementations, the parametric concept resides on varying a reactance, either inductive or capacitive. In this manner, while transconductance amplification relies on modulating the injection of energy from a DC source into the load, in the parametric technique, the amplification comes from periodically pumping a nonlinear device synchronised with an input signal. This is classically exemplified by the following analogy. If a mechanical force periodically modulates the distance, *d*, between the plates of a capacitor, its available total charge is periodically augmented and reduced. When at its peak the capacitor is discharged and pumps the circuit coherently, gain is possible. The effect of the mentioned applied force is analogous to modulating the capacitance by a pump signal. Accordingly, the amplification is achieved by delivering energy to the load from an AC power source through the nonlinear element. Since the principle is also valid for the resulting mixing products, it can also be applied to perform frequency conversion accompanied with amplification, and without DC power consumption. Therefore, prior to solid-state amplifiers and frequency converters based on devices suitable for high frequencies, these transistor-free designs were employed instead. It was not until the consecutive development of MOS processes that the use of transconductance-based designs boosted.

Nowadays, however, two factors occur simultaneously. The continuous scaling of transistors degrades their intrinsic gain, and new technologies and devices have become available to frontend designers. Both aspects favour the investigation of alternative approaches, and consequently, a renewed interest in parametric techniques has flourished, especially in the microwave and millimetre-wave domains [9]-[13]. Yet, these new approaches are still at their infant stage, and need to overcome several challenges that limit their performance, especially in integrated implementations, crucial for circuits working at high frequencies.

Due to the demand of high-speed wireless communications interconnects in wireless chip-to-chip communication, research is focused on transceivers suited for the mm-wave band and beyond for such applications. Since a decisive characteristic to design suitable frontends is low power consumption, the parametric technique is a promising candidate for such applications. Furthermore, the principle can be suitable for emerging technologies that lack of transistors but other devices with a promising variable-capacitance behaviour [13], e.g., graphene.

Nevertheless, the conventional varactor approach has, until now, presented several drawbacks for both upconverters and downconverters. For the former, the implemented designs so far irremediably required external circulators and duplexers, consequently, failing to provide a fully on-chip solution. Furthermore, the reported results are limited in bandwidth, require high local oscillator (LO) powers, or present low linearity. For the latter, the downconverters require a pumping signal that is higher in frequency than the input signal of interest for it to be either amplified or down-converted [13]. This is not suitable for high-frequency systems where the implementation of large-signal pumps becomes challenging. Thus, several analyses based on the nonlinear characteristics of varactors have been carried out recently to overcome these difficulties in standard and emerging technologies. Yet, these have

been only theoretically studied and besides the work in [14], the latest implementations date back to the 1950s. In both cases, the reason for the lack of success in this approach relies in the choice of the nonlinear device that is limited to the reversed bias region, and the topology employed for the circuit.

In the WiPLASH project we have carried out a revised analysis of the parametric concept to overcome these constraints and realise a direct up-conversion mixer at 60 GHz and a subharmonic down-converter from 57 GHz to 10 GHz. The modified concept is based on a nonlinear admittance rather than just a nonlinear reactance, and, in this manner, for the first time, a parametric-based up-converter could be successfully realized fully integrated and, additionally, by exploiting the highly nonlinear capacitance of a diode-connected heterojunction bipolar transistor (HBT), a subharmonic mixer that reaches positive transducer gains is achieved. Although tailored and dedicated to frontends based on graphene devices, this analysis and implementation was carried out by using a commercial SiGe HBT technology, as the available graphene MMIC technology with devices at high millimetre or THz frequencies was not stable enough for such a design. Also, the frequency range was chosen in such a way that measurements could be carried out easily in our laboratory. Therefore, the 60-GHz range was chosen without lack of generality of this approach and the possibility to port the design to the graphene-based MMIC technology.

3.1 The fully integrated parametric upconverter

The need of high-quality selective filters makes the implementation of on-chip parametric circuits challenging, and most of the times at least one circulator is required. In order to ease the monolithic integration, we propose the topology in Figure 15. The circuit consists of a double-balanced ring mixer, as used in passive resistive converters, which is adapted in order to apply a bias voltage to each diode pair. The four diodes are conformed by the connected collector-emitter HBTs, $D_{1\text{-}4}$. The LO power is fed by means of a balun into the core of the circuit, while the output RF is obtained through a second balun. Meanwhile, the IF is applied at the centre tap of the latter through a lowpass configuration formed by capacitors C_{IF} and the inductor L_{IF}. In addition, in order to apply a DC bias voltage, four resistors, $R_{1\text{-}4}$, are placed at the terminals of each diode such that D_1 and D_4, and D_2 and D_3, are biased at V_1 and V_2, respectively, and capacitors $C_{1\text{-}4}$ separate the different bias conditions. Finally, four decoupling capacitors, $C_{decap,1\text{-}4}$ are integrated on-chip as well to fully isolate the DC from the RF paths. The applied bias voltage is crucial for the circuit to work for two reasons. First, it selects the quiescent point of the diodes, selecting the optimal working point, such that the needed LO power is minimal for maximum capacitance variation. Second, it compensates the asymmetry of the diodes at each polarity and fixes possible imbalances that might degrade the overall performance. This topology intrinsically isolates the LO from the IF and RF, while the last two are more easily isolated due to their big frequency difference.

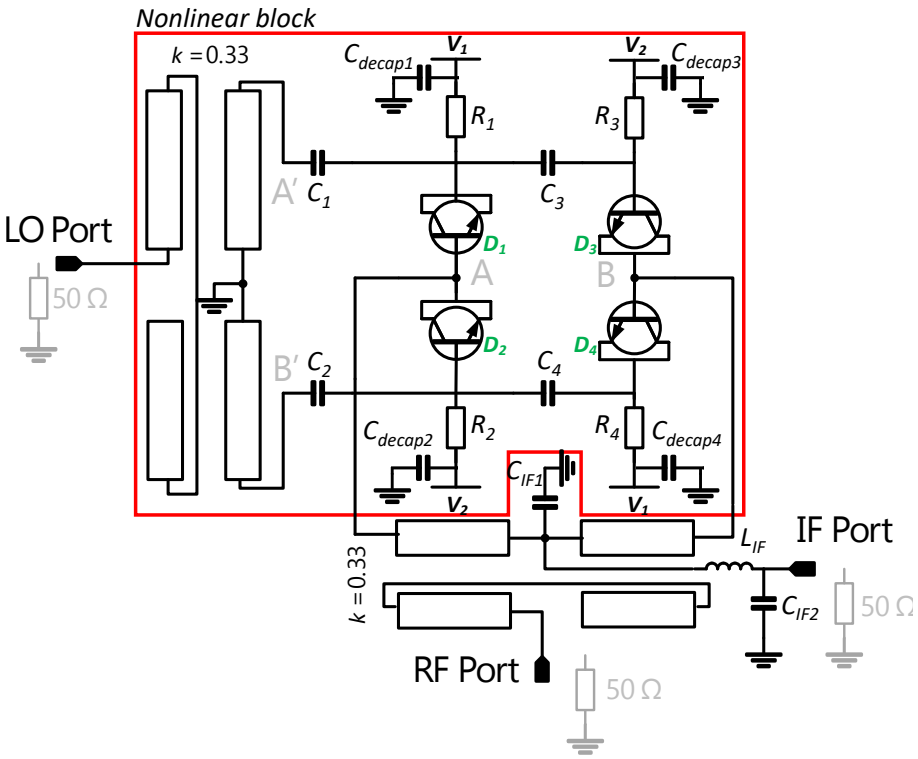


Figure 15 Schematic of the implemented circuit. The value of the lumped components in the double-balanced topology is: $C_{decap,1,2,3,4}$ = 4 pF, $R_{1,2,3,4}$ = 2 kΩ, $C_{1,2,3,4}$ = 2 pF, $C_{IF,1,2}$ = 0.2 pF, and L_{IF} = 170 pH.

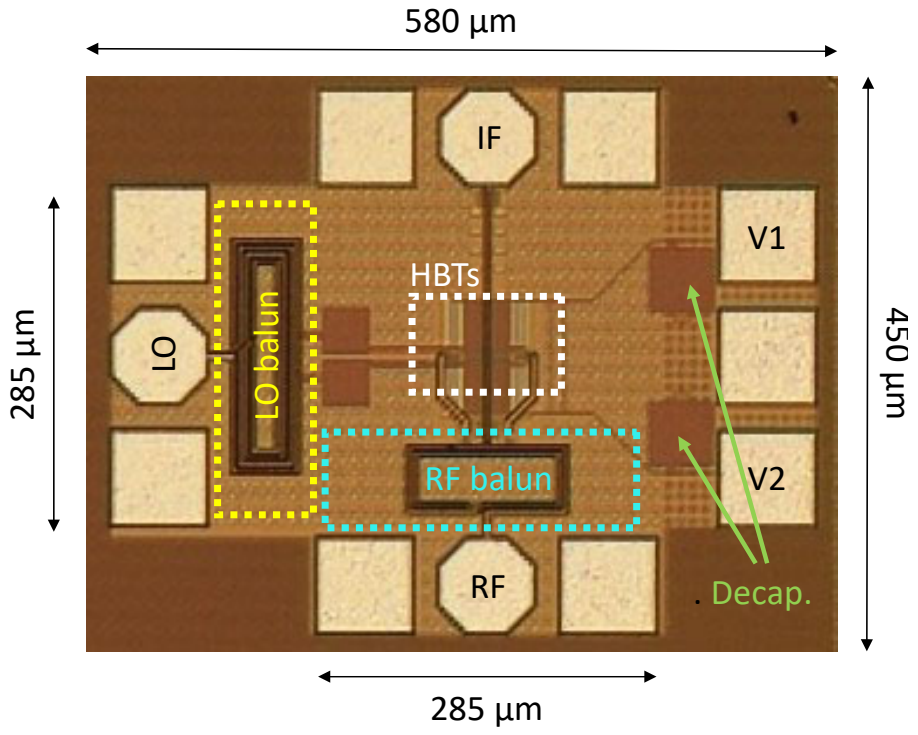


Figure 16 Micrograph of the parametric upconverter. The total occupied area, including the pads, is 0.261 mm²

A photo of the fabricated parametric upconverter is shown in Figure 16. The total occupied area, including the pads, is 0.261 mm² and thanks to the input and output

baluns, no further external filtering is needed. In order to fully characterize the performance and validate the elaborated models and theory, three setups are considered in the measurements. Initially, the network analyzer (NA) PNA-X is used as LO and IF source, and its spectrum analyzer mode is employed as readout. In this manner, all ports present a standard load value of 50 Ω and the impedance seen by the diodes is given by this value together with the impedance imposed by the implemented baluns. Additionally, in order to achieve the desired LO power sweep an amplifier is placed directly on the LO probe between the NA and the circuit. The bias voltage is applied by two independent DC sources that are also used to monitor the current consumption.

The measured output power and conversion gain over input IF power, LO power, and IF frequency under an applied voltage of 1.1V at V_1 and 0.89V at V_2, are presented in Figure 17. A maximum conversion gain with an applied LO power of 12.7 dBm of 1.5 dB is obtained and the 1-dB compression point is -8 dBm. From Figure 18 it can be seen that gain is achieved for LO powers greater that 7 dBm for a -12 dBm IF input. In both plots, the simulated and Verilog-A modelled outputs are compared showing good agreement with the measurement results. The best accuracy is obtained with the original PDK model of the transistor, while a similar performance of the programmed model proves the validity of the extracted parameters and the studied working principle of the parametric device. Figure 19 shows the behaviour of the parametric upconverter over a sweep of IF frequencies. A sort of bandpass conduct is observed, where the best performance is observed at 0.7 GHz. The extracted 3-dB bandwidth of the filter is around 5 GHz and 4.7 GHz for the USB and LSB, respectively, and gain is achieved over a bandwidth of 2 GHz.

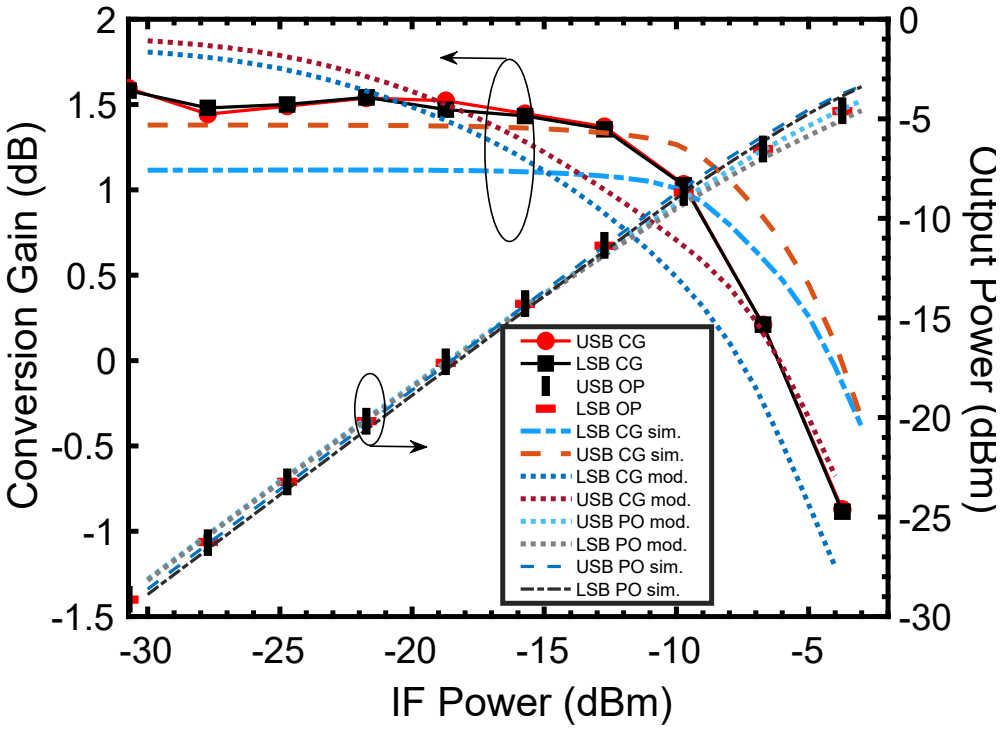


Figure 17 Conversion gain (left axis) and output power (right axis) over input IF power

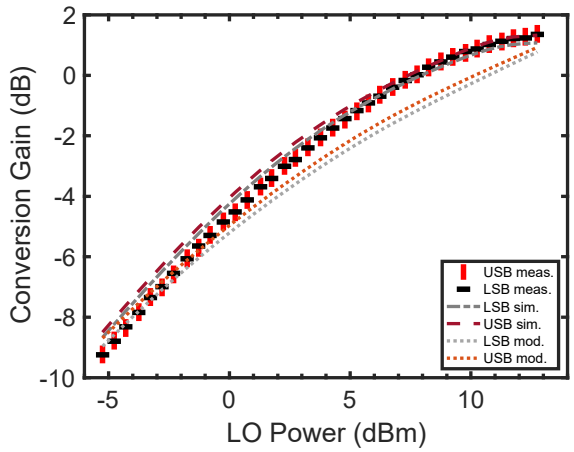


Figure 18 Conversion gain over LO power

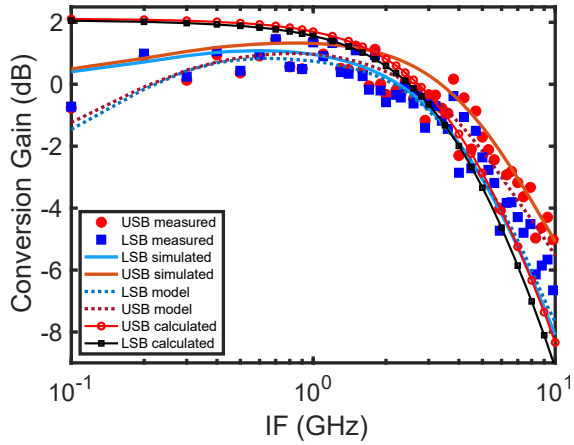


Figure 19 Conversion gain versus IF

In Figure 20, the RF-to-LO isolation is shown over the applied LO power for a -12 dBm IF signal. It is observed that the isolation improves for higher LO powers and achieves up to 53 dB for an LO of 12 dBm. The increasing effect is due to the improvement of the matching between the diode pairs, so that the best balance is achieved for higher LO powers for the applied bias voltage. The baluns have been optimized in terms of occupied area. An improvement on the coupling and balance over a wide range of LO powers of the input balun could improve the overall performance, including the isolation at lower powers. Furthermore, because the diodes are biased at their conduction edge, for at least half of the LO cycle there is current flowing through them, which translates into DC power consumption. The large capacitance variation, which allows the gain of the circuit, comes at this cost, but the extracted value is very low and equals 0.618 mW as calculated from the measured currents and plotted. In the plot, it can be seen that the current increases with the increase of LO power, according to theory. This is also the case with the increase of IF power, when the amplitude can no longer be considered small, and it starts to modulate the admittance.

To further characterize the linearity, a second setup is used to measure the third-order intermodulation products. An additional clean source is employed as IF input, and a broadband Wilkinson power divider is chosen to combine both IF signals. The measured results for an input LO power of 12.75 dBm and frequencies of 700 MHz

and 750 MHz are plotted in Figure 21. The observed IIP_3 is -4.57 dBm, while the OIP_3 is 4.7 dBm.

Finally, in order to verify the impact of the impedance seen by the diodes at each frequency, to the first described setup, a mechanical impedance tuner is added between the IF port of the NA and the circuit. The measured results are shown in Figure 22 for an applied voltage of -0.9 V and 0.84 V. From Figure 22, it is observed that under the new conditions, gain has increased up to 4.75 dB for a -20-dBm IF input, and up to 3.9 dB for a -10-dBm IF input, both at 700 MHz and that gain is already achieved for a -1-dBm LO signal. However, as shown in Figure 23 the 3-dB bandwidth is limited to 20 MHz, while gain is achieved over around 30 MHz. This effect agrees with the narrow bandwidth of the impedance tuner. Unfortunately, the tuner is not suited for the RF frequency range in use, and the same strategy cannot be applied for the RF port. It is interesting to highlight that despite the increase of the gain, power consumption does not increase since it is only dependent on the powers applied to the LO and IF, and the quiescent point determined by the DC bias. The maximum measured DC power consumption for the -10-dBm IF is at the maximum applied LO and equals 0.4 mW.

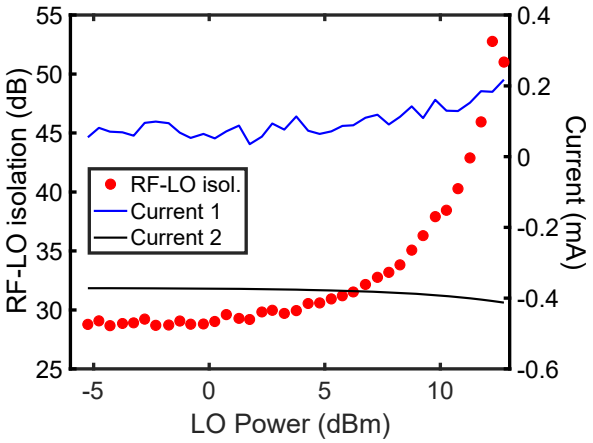


Figure 20 RF-LO isolation (left axis) and current measured from both DC sources over applied LO power

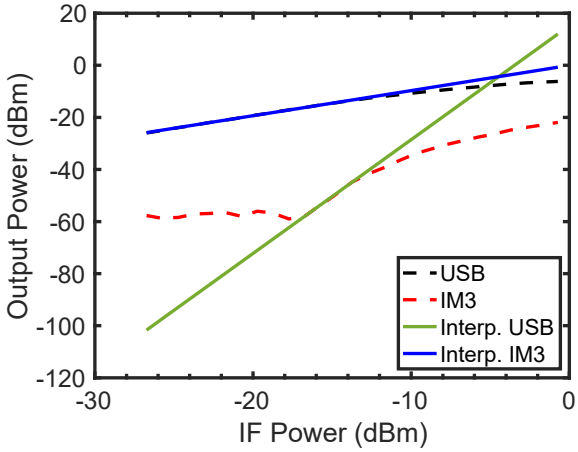


Figure 21 Third order intermodulation products measurement results. In dash lines, the fundamental and IM_3 output power. In continuous lines, the linearly interpolated output. The intersection indicates the IIP_3 (x-axis) and OIP3 (y-axis).

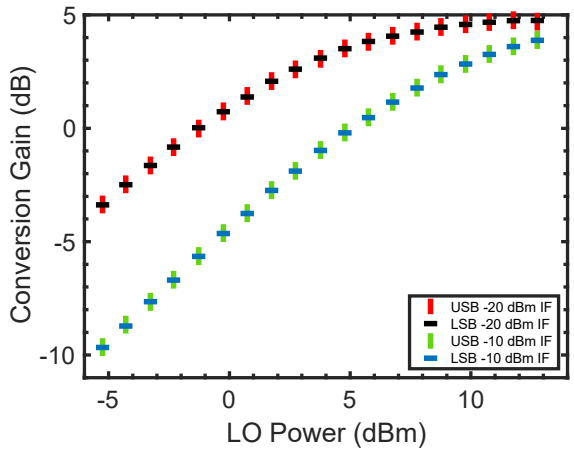


Figure 22 Measurement results for the third setup, after adding the impedance tuner at the IF output. Conversion gain over applied LO power

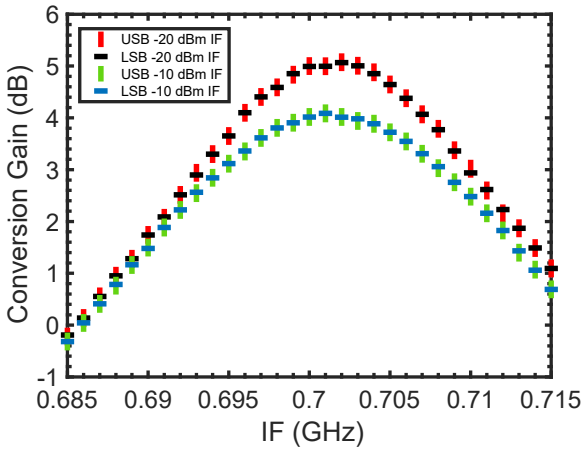


Figure 23 Measurement results for the third setup, after adding the impedance tuner at the IF output. Conversion gain over IF

3.2 The subharmonic parametric downconverter

For a subharmonic downconverter, the terminated product of interest is the intermediate frequency (IF), f_{IF}, that equals $2f_{LO}$-f_{RF}. It should be noted that it is assumed here that the allowed frequencies are f_{LO}, $2f_{LO}$-f_{RF}, and f_{RF}, as shown in Figure 24. Despite the subharmonic pumping the power of the second harmonic ($2f_P$) is not embraced, *i.e.* the second coefficient, C_2, is responsible for the subharmonic down-conversion and not the harmonic frequency component itself. Thus, the first requirement is the use of a device with a sufficiently high C_2/C_0 ratio.

Contrarily to upper sideband upconverters the maximum conversion gain of lower sideband upconverters and downconverters is not limited by the Manley-Rowe energy relations to the frequency ratio f_{out}/f_{in} [2]. A negative input conductance can be inferred in the diode by the effect of the pump on the variable capacitance. Consequently, the transducer gain can be made arbitrarily large by adjusting the bandwidth and tolerated sensitivity, where the latter is defined as the fractional change in the gain divided by the fractional change in the parameter affecting the gain [2]. These conditions indicate that impedance matching at the RF (signal) and IF (idler) ports is not possible and that the circuit is potentially unstable, yet they provide flexibility in the design and enable high-gain parametric downconverters. Since all these statements also hold true for

subharmonic converters where $f_{RF} = 2f_{LO} – f_{IF}$ [13], we could show how it is possible to exploit these properties when a highly nonlinear device (high C_2/C_0) is properly pumped and biased. In this circuit implementation the nonlinear element is a 10-finger diode-connected HBT (with emitter width and length of 70 and 900 nm, respectively) where also the two terminals are the base and the shorted collector-emitter pair, as depicted in Figure 24. The extracted coefficients over the LO amplitude and bias voltage are shown in Figure 24. It is observed that when maximizing C_2 at the edge of conduction the required LO swing is lower; thus, the pump power requirements can be relaxed for quiescent points around 0.8 V.

The schematic of the implemented parametric-based mixer is presented in Figure 25. It consists of a modified four-diode double-balanced topology, where instead of a balanced RF input, to allow the odd mixing products, the RF signal is applied in-phase to the two diode pairs D_1-D_2 and D_3-D_4. The pump signal enters the circuit through an integrated balun designed at 35 GHz so that the balanced signals cancel the odd LO harmonics while the antiparallel diode pairs D_1-D_3 and D_2-D_4, as in a double-balanced mixer, cancel the even ones, hence, avoiding the use of on-chip filters. As shown in Figure 26, the LO balun is implemented in the thick top-most back-end-of-line (BEOL) layers to minimize the ohmic loss. Additionally, a DC biasing path is provided to each diode polarity through resistors R_{1-4} and the on-chip decoupling capacitors C_{1-4} in order to select the quiescent point of the transistors and facilitate the tuning to maximise the conversion gain. Because both the input and idler signals are in-phase the transistors are effectively in parallel to the IF and RF ports, hence, it can be assumed that the embedding impedance seen by each transistor is four times the common-mode impedance at nodes A, and B, as shown in Figure 26. Accordingly, the circuit can be analysed as a single-diode parametric mixer. Since, as already stated, matching is not possible when a negative conductance is induced, the RF and IF paths are designed to be resonant at the frequencies of interest under the properly chosen LO power and DC voltage to maximize gain. As shown in Figure 25, the resonant tank is formed by the RF port input transformer and a shunt transmission line that is connected to the centre tap and capacitor C_5 that connects to the output IF port.

To characterize the gain performance on-chip measurements are carried out. The measurement setup consists of the network analyzer, which is used as an RF source and as a receiver at the output port, two DC voltage sources that are used for the two different applied bias voltages, and an external LO source as shown in Figure 27. The LO source is calibrated with a power sensor and the cable losses are de-embedded from the measurements by characterizing their *S*-parameters. Since the output port is left without further filtering to demonstrate that the induced input negative conductance appears at both the RF and IF, both signals appear amplified at the output, and the circuit demonstrates the possibility of achieving parametric subharmonic down-conversion to the IF and amplification of the input signal. Thus, both gains are characterized over RF input power and LO input power, as depicted in Figure 28. For an RF input of 57.3 GHz and an LO of 33.7 GHz and 6.3 dBm the gain at the 10.1 GHz IF and the RF are practically the same, and around 14 dB while the OP_{1dB} is about -33 dBm. As expected from the measured high gain, the performance over LO input power shows a high sensitivity to changes in the pump. Beyond 6.7 dBm LO power, the circuit becomes unstable and two spurious oscillation signals appear in both bands, IF and RF. Furthermore, the high sensitivity is also coherent with the measured narrow IF bandwidth of 20 MHz, shown in Figure 29, for an LO power of 6.2 dBm. On the other hand, the RF bandwidth, when fixing the IF to 10.1 GHz and tuning the LO accordingly,

reaches up to 300 MHz, as shown in Figure 29. The quiescent points for these measurements are V_1=-0.813 V and V_2= 0.805 V. Since this is the edge of conduction of the diode-connected HBTs, where nonlinearity is maximum, a small DC current is driven. However, the maximum DC power consumption is as low as 235 µW. It should be noted that the amplifier is also a reflection amplifier or non-degenerated negative-resistance amplifier, where the power of the reflected signal at the RF port is also amplified. This can also be characterized by the reflected wave in the VNA. In optimized designs, this needs to be considered by including an isolator at the input or modifying the topology to use the needed hybrids. The photograph of the implemented prototype parametric subharmonic converter is shown in Figure 30. The fabricated prototype occupies a total chip area including the probing pads of 0.36 mm^2.

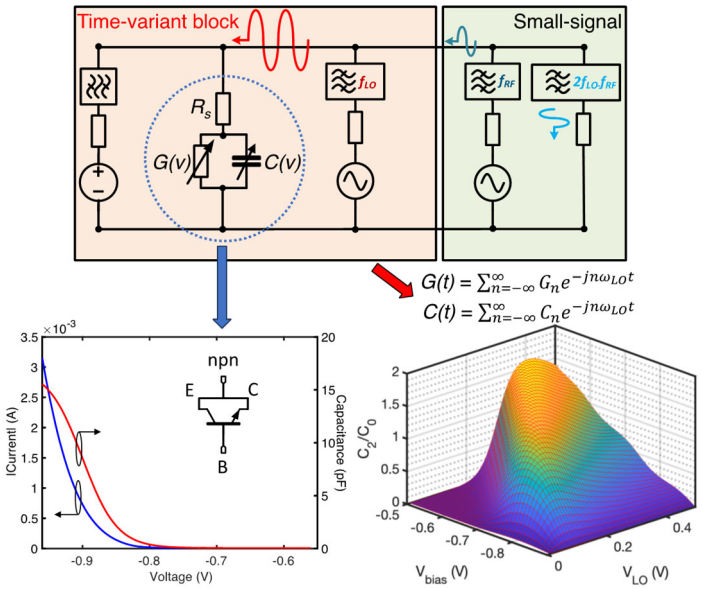


Figure 24 Parametric concept showing the nonlinear characteristics of the diode-connected HBT

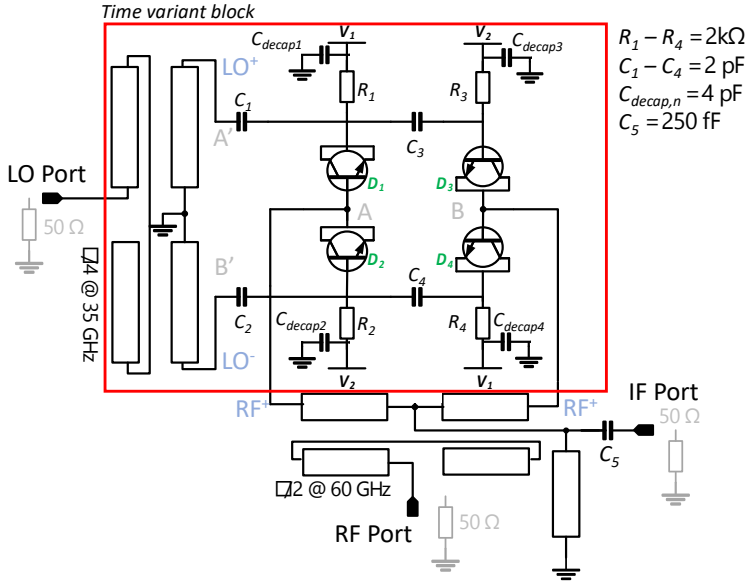


Figure 25 Schematic of the implemented subharmonic parametric downconverter prototype

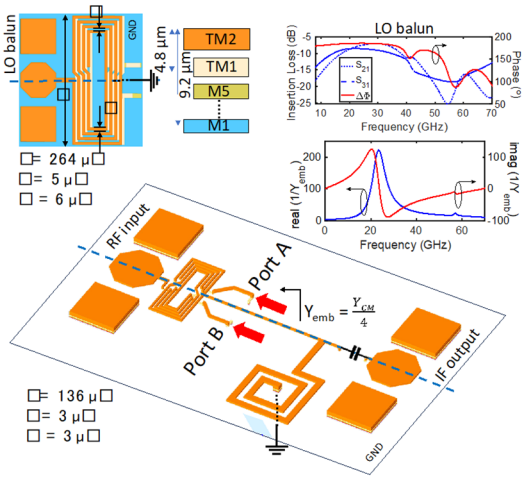


Figure 26 Diagram of the implemented LO balun with its insertion loss and phase difference, and the resonant structures of the RF and IF ports with the embedding impedance presented to each diode

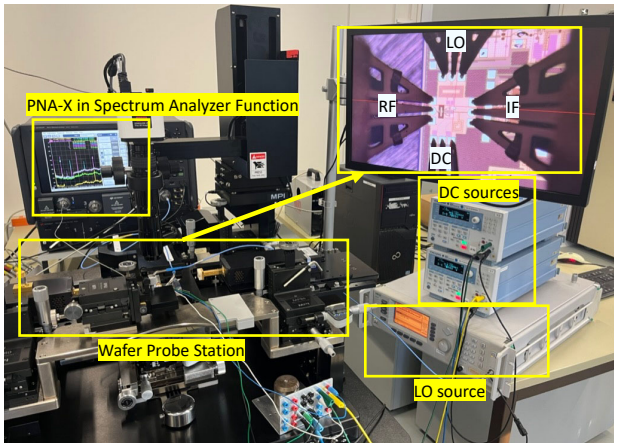


Figure 27 Prototype characterization setup for the conversion gain measurements. The Network Analyzer is used as RF source and receiver in Spectrum Analyzer mode

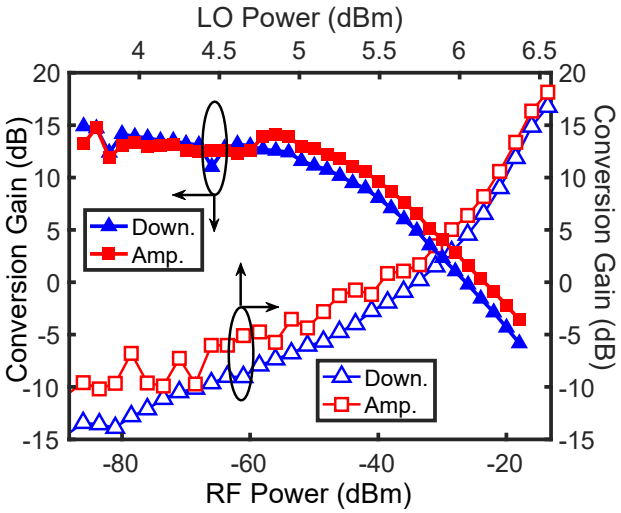


Figure 28 Measured conversion gain versus RF power with 6.3 dBm LO input power, and versus LO power and -56 dBm RF power

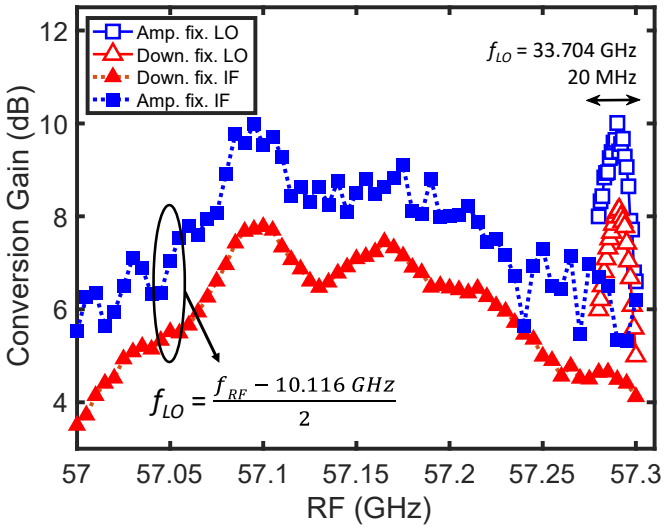


Figure 29 Measured conversion gain versus IF bandwidth and RF bandwidth for an LO power of 6.2 dBm and an RF power of -56 dBm.

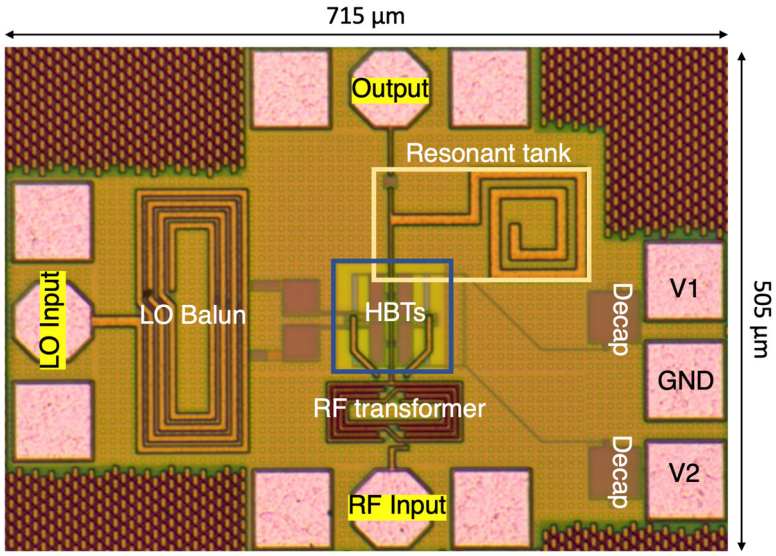


Figure 30 Chip micrograph of the fabricated prototype occupying 0.715 mm x 0.505 mm

4 Graphene diode-based Communication Transmitter

The design of RF transmitters (Txs) using MIG diodes on flexible substrates is presented. This is achieved by utilising an MMIC process. The circuits are fully integrated and fabricated on PI substrates. An RF transmitter is a device that generates an RF signal and transmits it through an antenna. The signal can be modulated to carry information such as audio, video, or data. The signal is transmitted in the air to an RF receiver, which demodulates the signal and converts it back into its original data. RF transmitters are used in a wide variety of applications, including radio and television broadcasting, wireless communication devices, and industrial control systems. In traditional RF transmitters, a mixer circuit is used to convert the baseband or intermediate frequency (IF) signal with a local oscillator (LO) signal to produce an RF signal, which is then further amplified and transmitted. Superheterodyne and homodyne Txs need an RF power amplifier which should be highly linear in order to not distort complex modulated signals. The RF PA however is currently very difficult to realise in emerging technologies, *e*.g., graphene, MoS_2. One possible solution is to adopt new transmitter architecture to accommodate the limitations of these technologies. In this project graphene-based diodes were available and thus transceiver architecture based on diodes have been investigate for their application in chip-to-chip communication scenarios.

In mixerless transmitters the baseband signal is directly modulated onto the RF carrier frequency without going through an intermediate frequency and without utilising a mixer like in heterodyne approaches. A mixerless transmitter based on polar RF digital-to-analogue converters (DACs) has been proposed for orthogonal frequency-division multiplexing (OFDM) modulated signals in [19]. A digitally assisted and spurious-free direct carrier mixerless modulator based on the six-port correlator has been reported in [20].

Based on the operation principle, a mixerless Tx does not require many filters for image and harmonic suppression since there are no spurs generated in the highly nonlinear mixing process. Another important parameter to consider when designing with emerging technologies is typically the lack of sufficient gain at high frequencies. This is also the case for the available graphene devices especially the ones on flexible substrate.

Consequently, a four-way mixerless Tx architecture [21]-[23] is appropriate according to our current graphene technology.

The basic components of the proposed mixerless Tx are the power splitter at the input side, the power combiner at the output side, and impedance modulators. Figure 31 shows one of the proposed mixerless Txs which consists of 3 branch-line couplers (BLCs) as quadrature-phase power splitter at the input side, four MIG diodes as impedance modulators, and 3 BLCs as four-way power combiner at the output side. The power splitter and the power combiner can be realised in various ways, *e.g.*, branch-line couplers and transmission-line phase shifters in this design. The transmission lines, TL_1, TL_2, TL_3, and TL_4, are designed to provide a constant phase difference of 90° in order to be able to sum up the signals correctly at the output of the transmitter.

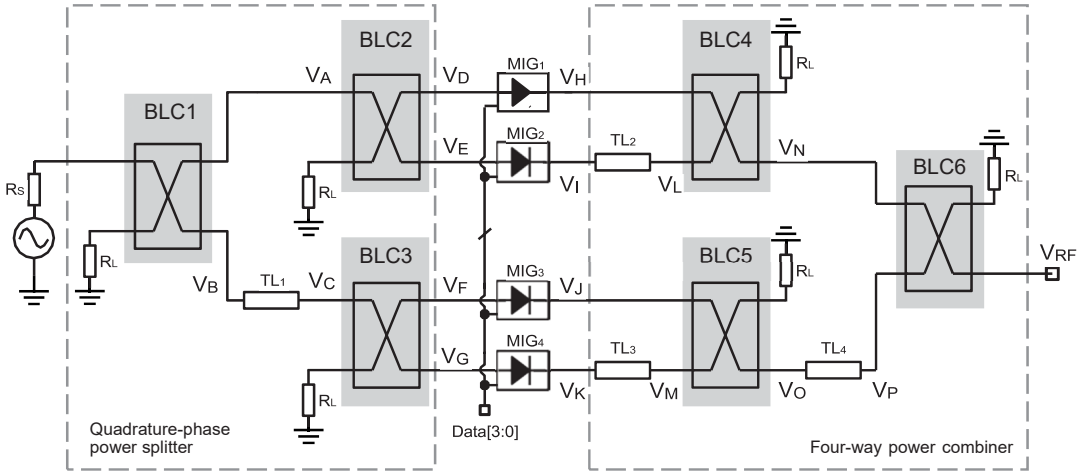


Figure 31 Block diagram of the proposed mixerless transmitter.

Keysight ADS is used to simulate and optimize the graphene-based mixerless Tx. Figure 32 shows the simulated 16-QAM constellation diagram using simulation results of the BLCs, phase shifters, and actual measured impedances of the MIG diodes. The applied two DC bias voltages of the MIG diodes are 0.1 V and 0.25 V, respectively, to acquire the 16-QAM symbols. EVM_{peak} of 5.61 % and EVM_{rms} of 4.16 % are obtained. The results strongly indicate the feasibility of the Tx on the available graphene MMIC process. Based on the study of the mixerless Tx concept, it suggests that there is more than one architecture to perform and to acquire such amplitude/phase relationships explained above. Thus, different types of architectures have been further investigated with the technical restrictions of the graphene MMIC process.

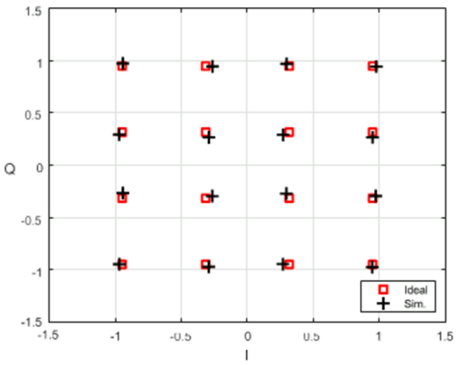


Figure 32 Simulated output 16-QAM constellation of the transmitter using measured impedances of the MIG diodes and other simulated components.

The first configuration as shown above employs the series MIG diodes leading to some difficulties implementing the bias networks especially with such low-Q integrated inductors. As a result, the shunt-MIG-diode configuration is preferable. In this section, the considerations of real implementation are comprehensively discussed. Three

2.4 GHz Tx configurations using shunt MIG diodes with actual bias networks and their corresponding layouts are shown later. The three configurations are proposed as follows:

1. **Approach I:** A Tx composed of three branch line couplers as the input network and three Wilkinson (WK) power dividers as the output network with microstrip-line (ML) implementation (TX:ML:3BLCs:3WKs).
2. **Approach II:** The Tx composed of one WK and two BLCs as the input network and three WKs as the output network (TX:lumped:2BLC:4WKs).
3. **Approach III:** A Tx composed of three WKs as the input network and three WKs as the output network (TX:lumped:6WKs)

Additionally, an experimental flexible Tx at 18 GHz has also been designed using microstrip lines to validate the high frequency scaling process.

4.1 Approach I: microstrip transmission line

A mixerless transmitter composed of microstrip lines is designed and simulated. Figure 33 shows the structure of Approach I. The quarter-wave transmission lines lead to amplitude imbalances in different paths due to the losses of the lines. Besides, more transmission lines also increase the size of the transmitter. Therefore, the Wilkinson power dividers instead of couplers as the output in the Approach I transmitter is employed.

Figure 34 shows the complete layout of Approach I Tx. The quadrature-phase power splitter is composed of 3 conventional microstrip branch-line couplers and the four-ways power combiner consists of 3 Wilkinson power dividers. The microstrip lines of the BLCs are meandered for a compact design. Four MIG diodes, the corresponding integrated bias networks and the measurement pads are also shown. The circuit occupies a chip area of 49.66 mm × 49.29 mm including the input, output, and bias probing pads.

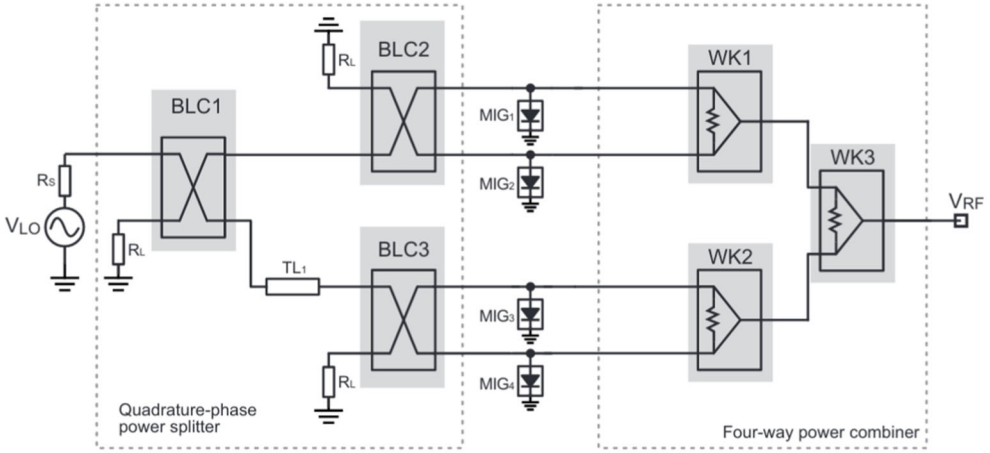


Figure 33 Block diagram of a mixerless transmitter based on microstrip lines (Approach I)

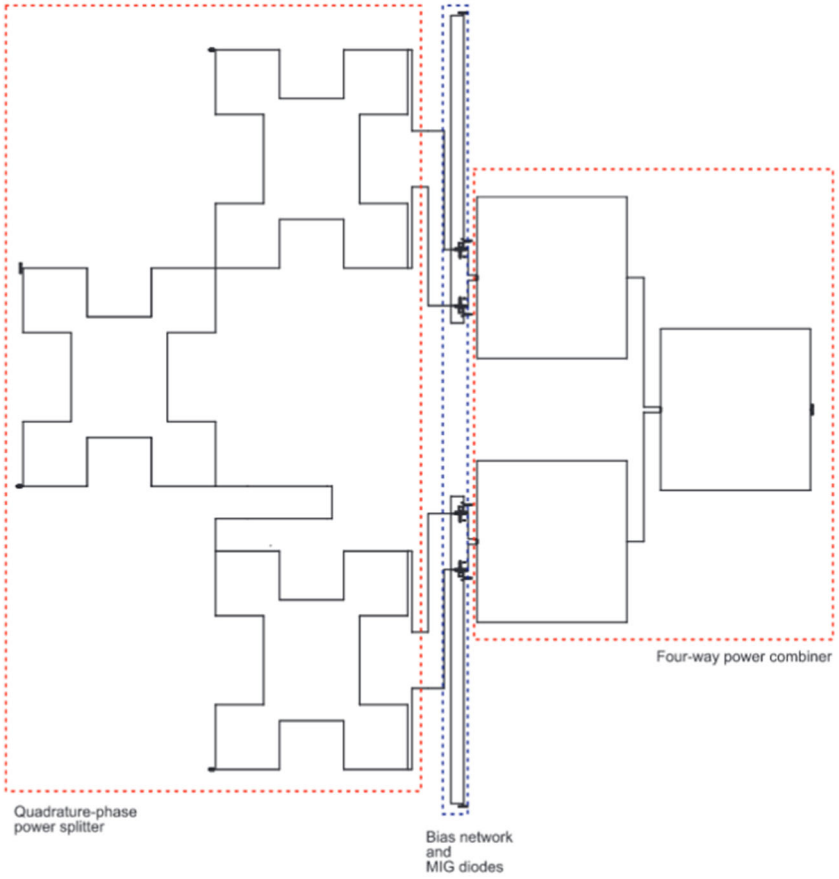


Figure 34 Complete layout of the Approach I transmitter.

The simulated S-parameters of the quadrature-phase power splitter are depicted in Figure 35. At 2.4 GHz the reflection coefficients, S_{11}, S_{22}, S_{33}, S_{44}, S_{55}, are all below −12 dB. The insertion losses, S_{21} and S_{31}, are both −14.0 dB and S_{41}, S_{51} are −16.7 dB. The reason for the different insertion loss is mainly due to the additional quarter-wave transmission line, TL1, at the coupling port, *i.e.*, Port 3 of BLC1.

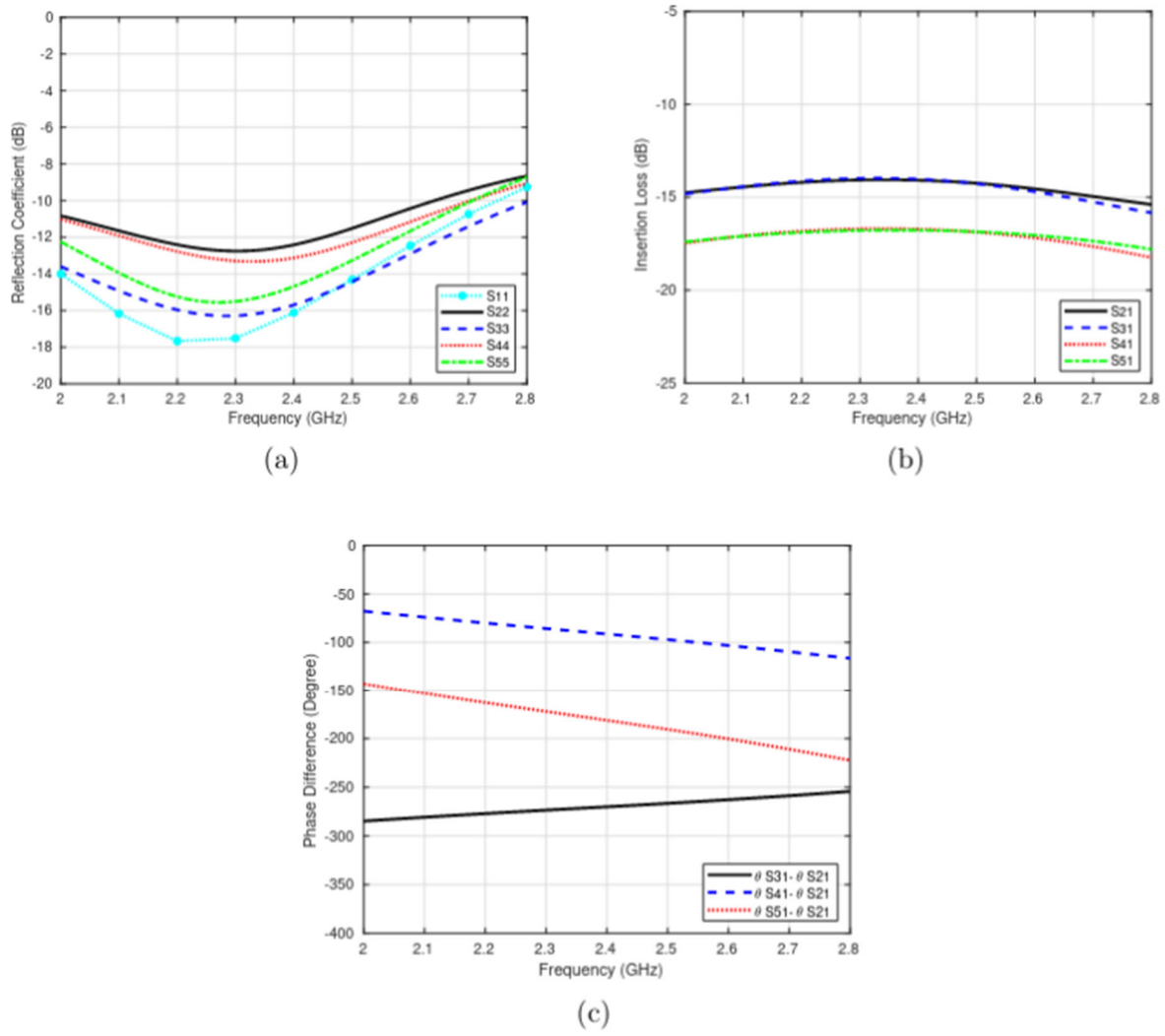


Figure 35 Simulated S-parameters of the power splitter for Approach I Tx: (a) reflection coefficient, (b) insertion loss, and (c) phase difference.

Figure 36 depicts the performance of the four-way power combiner. The reflection coefficient at 2.4 GHz is less than −16 dB as plotted. The insertion losses, S_{21}, S_{31}, S_{41}, S_{51}, are −12.7 dB. Figure 36 plots phase differences of S_{31}, S_{41}, S_{51} with respect to S_{21}. Phases of 0.0° are obtained in the simulation indicating that the layout of the four-way power combiner is highly symmetrical.

Another important subnetwork is the bias network used to provide appropriate DC bias voltages to the MIG diodes. Figure 37 shows the bias network. P_1 and P_2 are the RF ports and the RF signal can pass through. C_1 and C_2 are the DC blocks, that prevent the flow of DC current into the RF path. P_3 is connected to a DC voltage. L_1 is used as an RF choke to block the RF signal flowing to P_3. C_3 is a bypass capacitor connected between the DC port and ground. It is used to have a good RF ground and also to prevent ripple from the DC power supply entering the RF system.

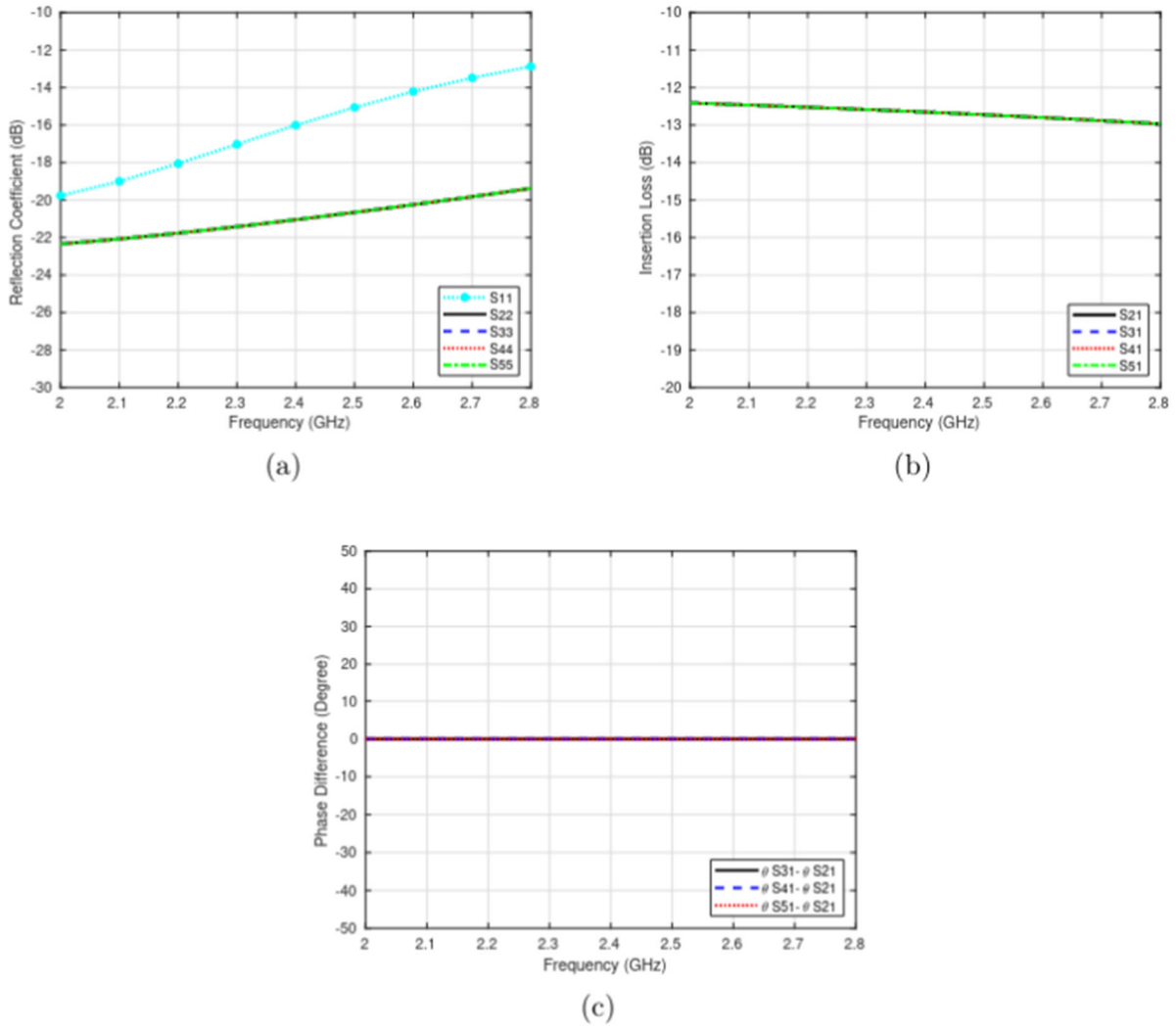


Figure 36 Simulated S-parameters of Approach I power combiner: (a) reflection coefficient, (b) insertion loss, and (c) phase difference.

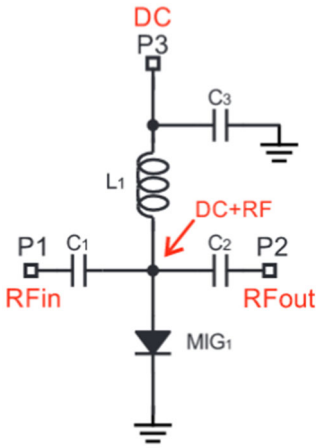


Figure 37 Schematic of biasing network for the MIG diodes.

The inductor, L_1, of 5.8 nH and capacitors, C_1-C_3, of 18.3 pF are employed and the layout of the bias network is shown in Figure 38. As can be seen the simulated insertion loss, S_{21}, is −4.2 dB at 2.4 GHz. Figure 38 show isolation, *i.e.*, S_{31} and S_{32}, of better than −45 dB, meaning that most of the RF signal does not flow to P_3, *i.e.*, to the DC port. To determine the bias voltages for 16-QAM, the EM-simulated bias network incorporated with the measured S-parameters of a MIG diode with different DC bias voltages are carried out. This hybrid simulation is performed to obtain more accurate results. Bias voltages of −1 V and 0.35 V are selected to obtain the minimum and the maximum $|S_{21}|$. Besides, −0.1 V is chosen to get the suitable attenuation for the 16QAM signal of the transmitter.

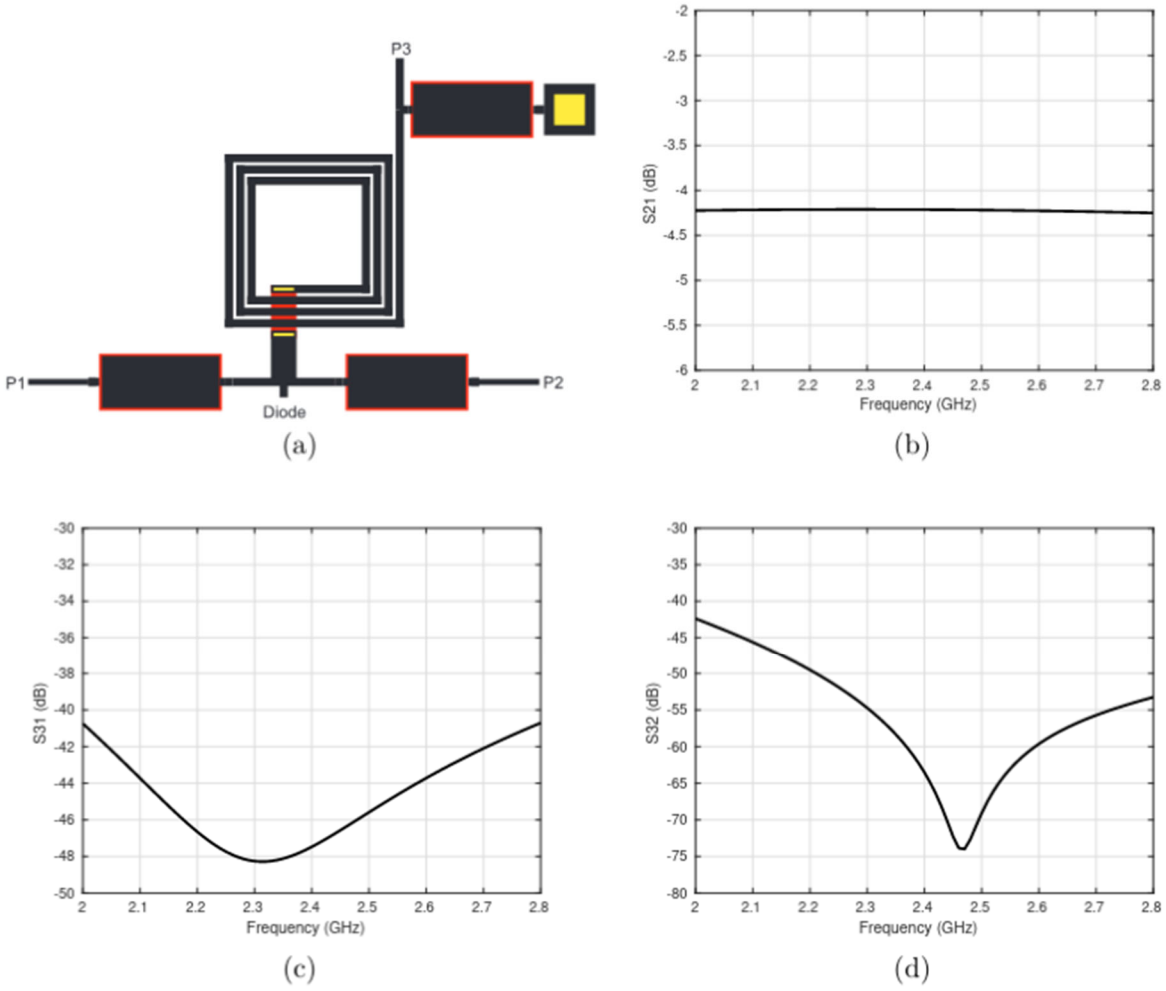


Figure 38 Biasing network operating at 2.4 GHz: (a) layout, (b) S_{21}, (c) S_{31}, and (d)S_{32}.

16-QAM is a modulation scheme that allows for transmitting data over a communication channel by modulating the amplitude and phase of a carrier wave. In this scheme there are 16 possible combinations of amplitude and phase that can be used to represent the 16 different symbols. The generated data stream is mapped to the corresponding symbols. Figure 39 shows a typical 16-QAM constellation diagram. Determining the correct bias voltages of the MIG diode is very critical to acquire a correct magnitude response of the MIG diode. Full EM simulation of the complete Tx

layout with the measured *S*-parameters of the MIG diodes taking the corresponding bias voltages is therefore performed.

A CW signal is fed to the input port of the Tx as LO signal. The simulated 16-QAM constellation of the Approach I Tx is plotted in Figure 40. The calculated EVM_{peak} is 7.80% and EVM_{rms} is 4.70%. Due to the physical dimension, a wafer-scale graphene process is required to fabricate this approach. The process is currently still under further development; hence a lumped-component approach has to be employed.

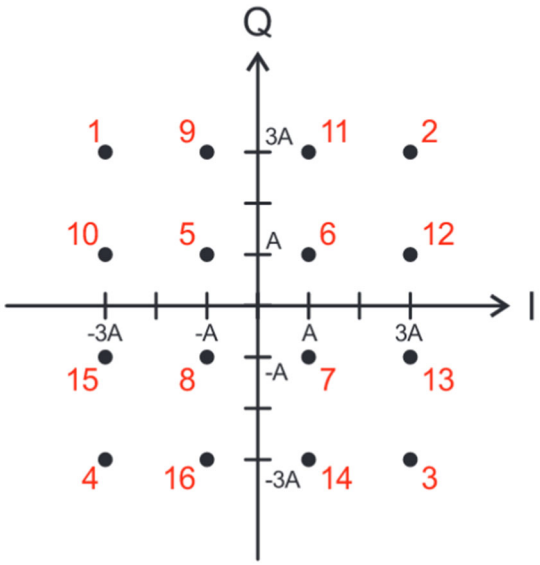


Figure 39 Constellation diagram for 16-QAM

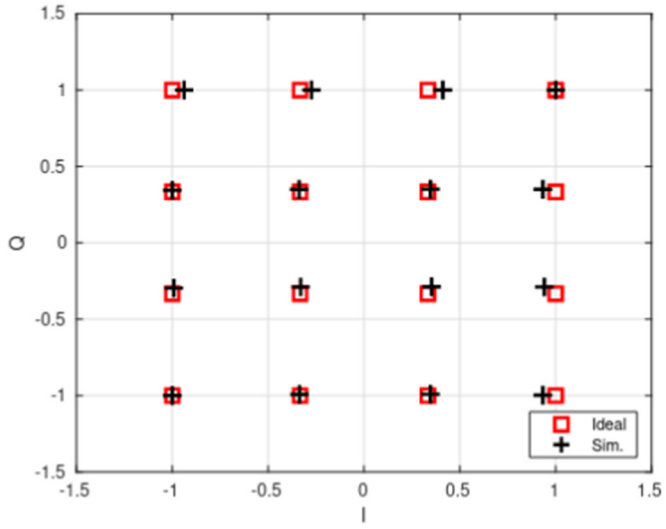


Figure 40 Simulated output constellation diagram of the Approach I Tx

4.2 Approach II: lumped

In this section, a compact transmitter, Approach II, is designed using lumped elements to realize phase shifters, couplers, and power dividers as shown in Figure 41. Compared to Approach I, Approach II is composed of one divider to replace one branch-line coupler in the quadrature-phase power splitter, because the measured performance of a lumped divider has been verified before.

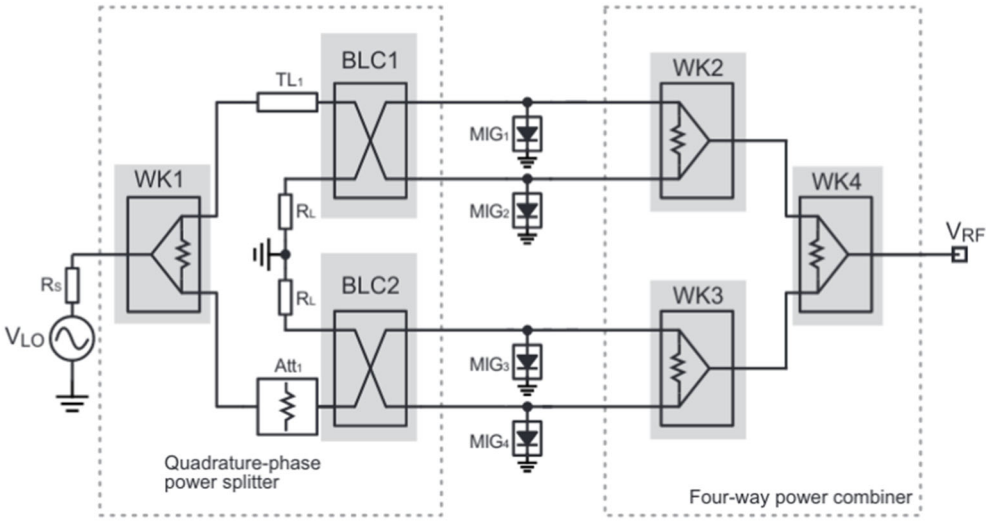


Figure 41 Schematic of a mixerless transmitter based on lumped components (Approach II)

To fulfil the phase differences between ports of the quadrature-phase power splitter, phase of the TL_1 has to be 180° instead of 90°. An attenuator, Att_1, is important and designed on purpose to compensate for the insertion loss of TL_1. A transmission line can be approximated using lumped components, *i.e.*, inductors and capacitors as an artificial transmission line. A 50 Ω 180° artificial transmission line can be divided into two 50-Ω 90° lines in a cascade. Such a quarterwave-length line is composed of the inductors $L_1 = L_2 = 3.32$ nH and the capacitors $C_1 = C_2 = C_3 = C_4 = 1.33$ pF, as shown in Figure 42. The two capacitors, C_2 and C_3, can be merged into a single 2.66 pF capacitor. The layout of the 180° artificial transmission line is shown in Figure 42. Figure 43 shows the simulated *S*-parameters of the transmission line. S_{11} and S_{21} are −25.1 dB and −1.9 dB at 2.4 GHz, respectively, and the simulated phase is −180.1° at 2.4 GHz.

The attenuator, Att_1, as shown in Figure 44, is designed to compensate for the −1.9 dB loss of the artificial 180° transmission line. The π-configuration attenuator consists of three resistors, R_1, R_2, and R_3 as shown in Fig. 44a. According to the theoretical calculation, resistor, R_1, is 8.1 Ω, R_2, and R_3 are 622 Ω. The values of the lumped-elements are L_1= 1.37 nH, C_1= 1.88 pF, and C_2= 1.33 pF. Metal layer M1 is used to realise the underpass. The quality factor of inductors is very low because of the thin metal layer M1.

In terms of performance the lumped-approach BLC is also comparable to the one with microstrip line. However, the size of the lumped BLC is 0.66 mm × 1.16 mm instead of 12.05 mm × 13.55 mm using the microstrip line resulting in a significant size reduction.

The different lumped parts for the Approach II transmitter are routed together and EM simulated. The complete layout is shown in Figure 45. The ground-plane is connected to the ground pads of all the GSG and GSSG pads. This makes a low-impedance reference plane for all circuit components. The Approach II transmitter occupies only a size of 6.5 mm × 4.1 mm. The simulated 16-QAM constellation is carried out in ADS and MATLAB and is depicted in Figure 46. The EVM_{peak} is 9.93 %, and the EVM_{rms} is 3.89 %.

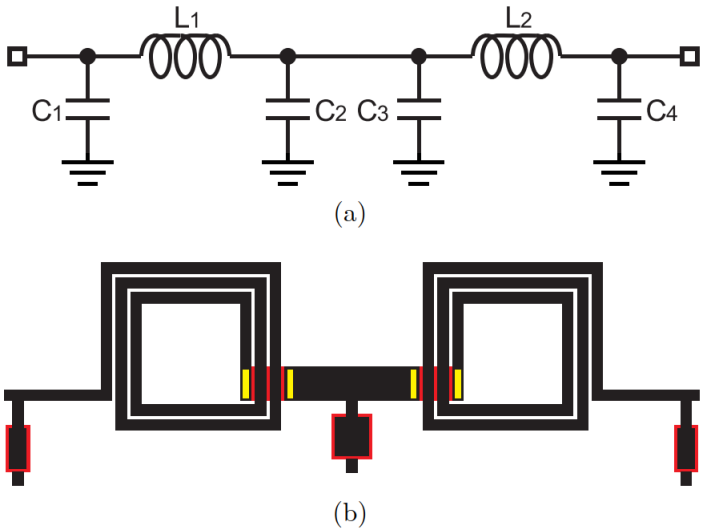


Figure 42 180◦ artificial transmission line: (a) Schematic and (b) layout

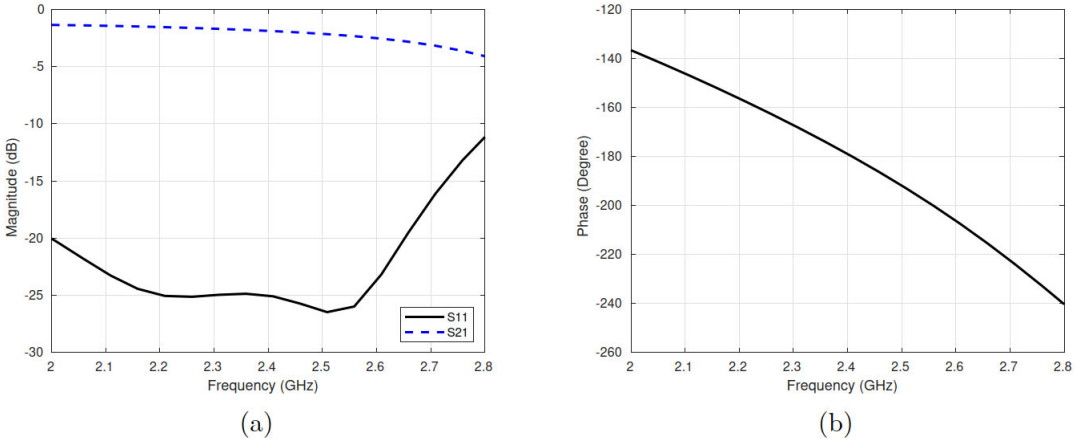


Figure 43 Simulated S-parameters of the 180◦ artificial transmission line: (a) magnitude and (b) phase characteristics.

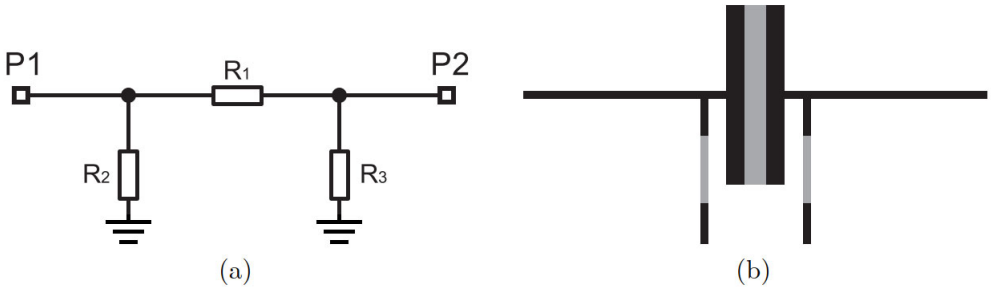


Figure 44 The designed π-type attenuator: (a) schematic and (b) layout

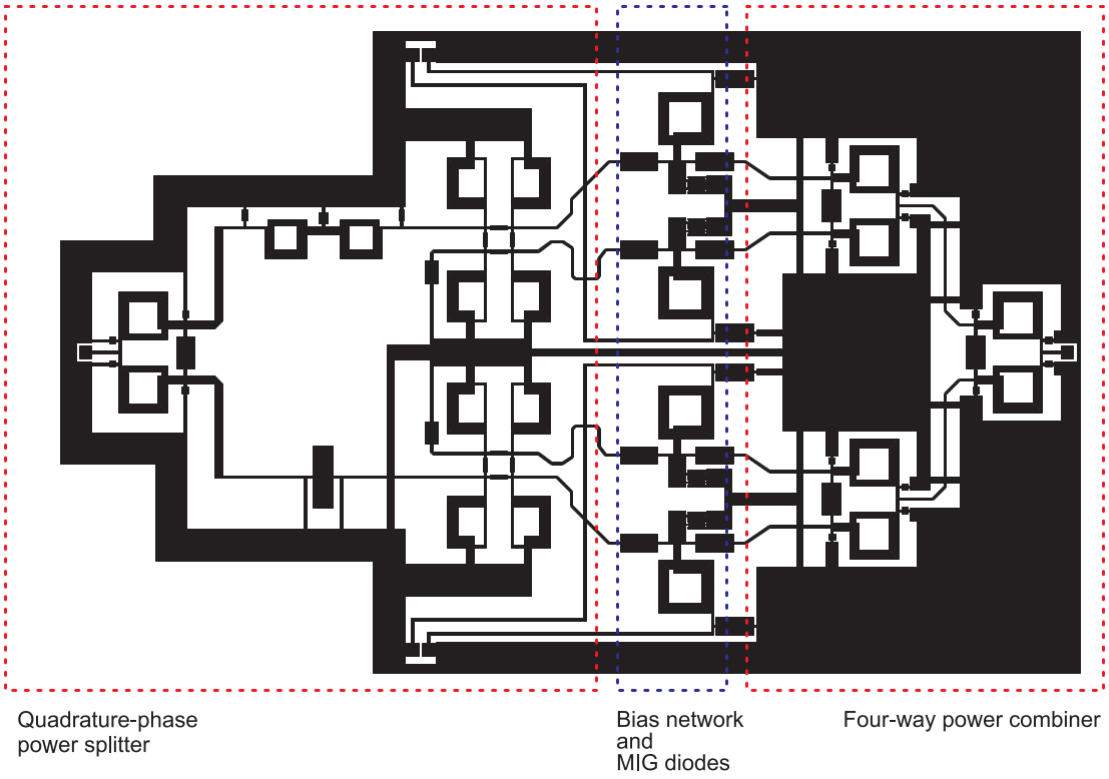


Figure 45 Complete layout of the Approach II transmitter

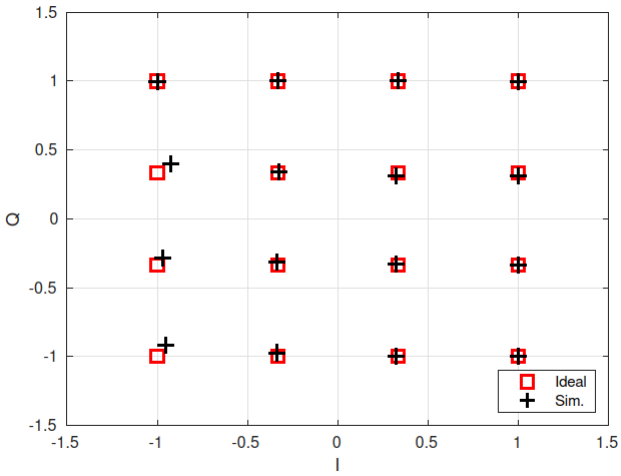


Figure 46 Simulated output signal constellation diagram of the proposed transmitter: Approach II

4.3 Approach III: all WKs

Approach III is another configuration for a lumped transmitter as shown in Figure 47 and it is also designed at 2.4 GHz. This transmitter is only composed of Wilkinson power dividers and lumped transmission-lines. The lumped Wilkinson power divider is desirable compared to lumped branch-line coupler, since the performance of the lumped Wilkinson power divider has been measured and verified. In Figure 47, TL_1=

220°, TL_2=TL_4=TL_6= 40°, TL_3=TL_5= 130°. Therefore, the phase difference of TL_1 and TL_2 is 180°. Note that TL_2 is added on purpose to balance the insertion loss of TL_1 as the same reason as the Att_1 in the Approach II. And the phase difference between TL_3 and TL_4 as well as TL_5 and TL_6 is 90°. The layout designed on the PI substrate is shown in Figure 48 with the size of 7.13 mm × 4.09 mm, which is similar to the size of Approach II. Figure 49 shows the simulated 16-QAM constellation of the Approach III transmitter. The simulated EVM_{peak} is 13.6% and EVM_{rms} is 7.7%.

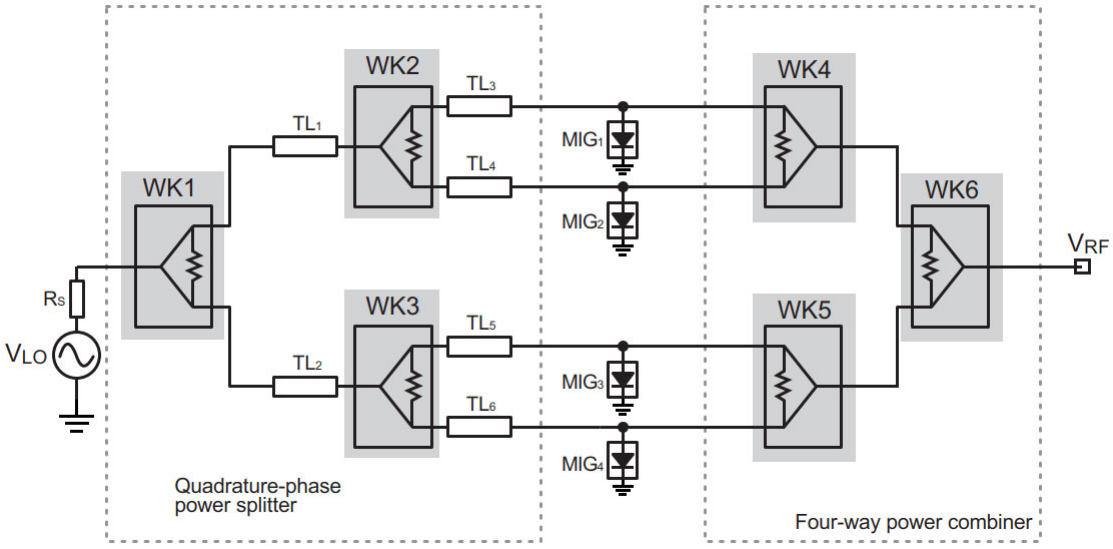


Figure 47 Schematic of a mixerless transmitter based on lumped WKs (Approach III)

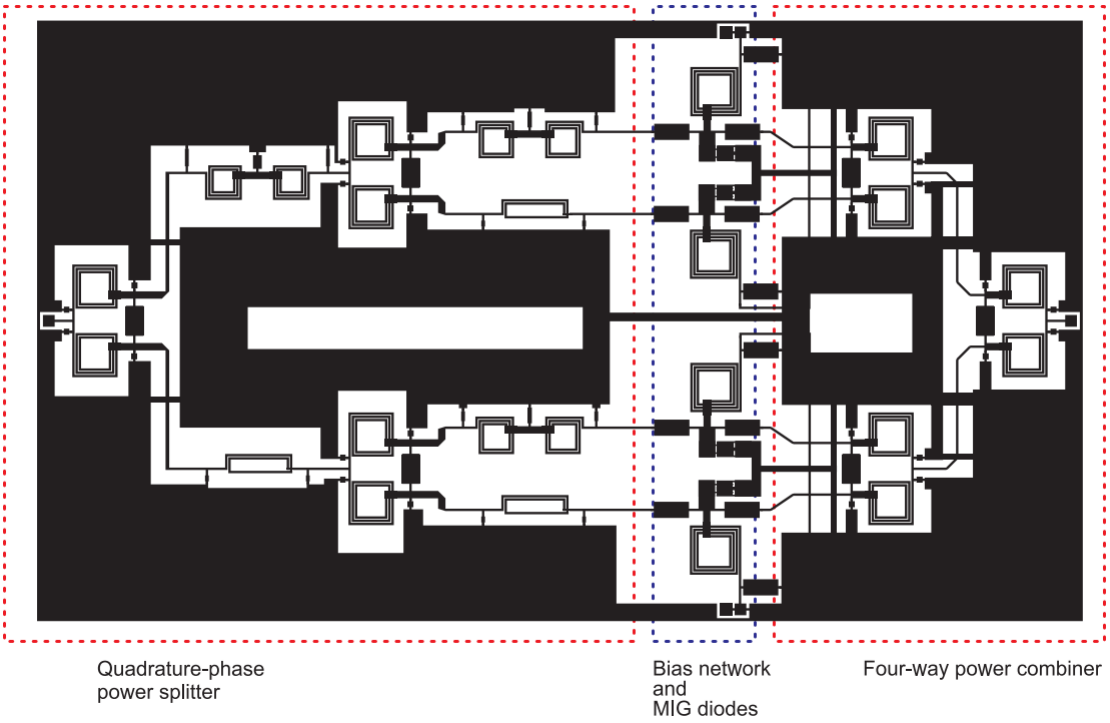


Figure 48 Layout of Approach III transmitter

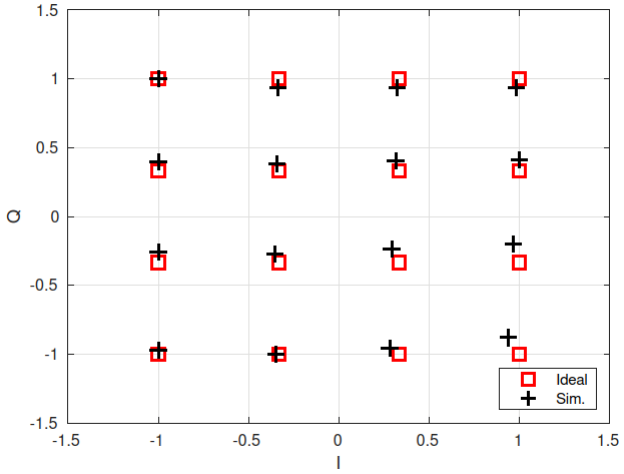


Figure 49 Simulated output signal of the proposed transmitter: Approach III

4.4 18 GHz Flexible Transmitters

The last design for the graphene flexible Tx is to make it reach the highest possible frequency and study its scaling feasibility. According to the measurements of the MIG diodes as well as the passive components, the highest possible frequency is 18 GHz for the available technology. Since the wavelength of 18 GHz is much shorter than at 2.4 GHz the lumped approach may not be suitable for this frequency. Therefore, the topology of Approach I is more suitable for higher frequencies. The layout of the 18 GHz Tx is shown in Figure 50 and the total size is 10.41 mm × 10.95 mm.

The simulated *S*-parameters of the quadrature-phase splitter is depicted in Figure 51. Figure 51a is the reflection coefficient. S_{11}, S_{22}, S_{33}, S_{44}, and S_{55} are all below −19 dB at 18 GHz. Figure 51b shows the insertion loss. S_{21}, S_{31}, S_{41}, and S_{51} are −8.6 dB, −8.7 dB, −9.2 dB, and −9.3 dB, respectively, at 18 GHz. Figure 51c shows the phase differences of S_{31}, S_{41}, S_{51} compared with S_{21}, which are 88.7°, −88.7°, −177.9°, respectively. The simulated 16-QAM constellation of the TX operated at 18 GHz is provided in Figure 52. The EVM_{peak} is 7.73% and EVM_{rms} is 4.32%.

4.5 Summary and conclusion

Four different Txs based on the mixerless Tx concept are shown here. These works demonstrate the possibility to fully integrate RF transmitters using the available graphene-based MMIC process on different substrates. The proof-of-concept Txs show the feasibility of transmitting 16-QAM modulated signals at 2.4 GHz and 18 GHz. Each of them has different bottlenecks and advantages. Therefore, the characteristics of the transmitters are summarised in Table 1.4. The designs have been taped-out and are currently in production.

Table 1 Summary of the graphene-based mixerless TXs

	Approach I		Approach II	Approach III
Main component	BLKs/WKs		BLKs/WKs	WKs
Implementation	microstrip-lines		lumped components	lumped components
Frequency (GHz)	2.4	18	2.4	2.4
Size (mm^2)	2447.7	114.0	26.7	29.2
EVM_{peak}(%)	7.8	7.7	9.9	13.6
EVM_{rms}(%)	4.7	4.3	3.9	7.7

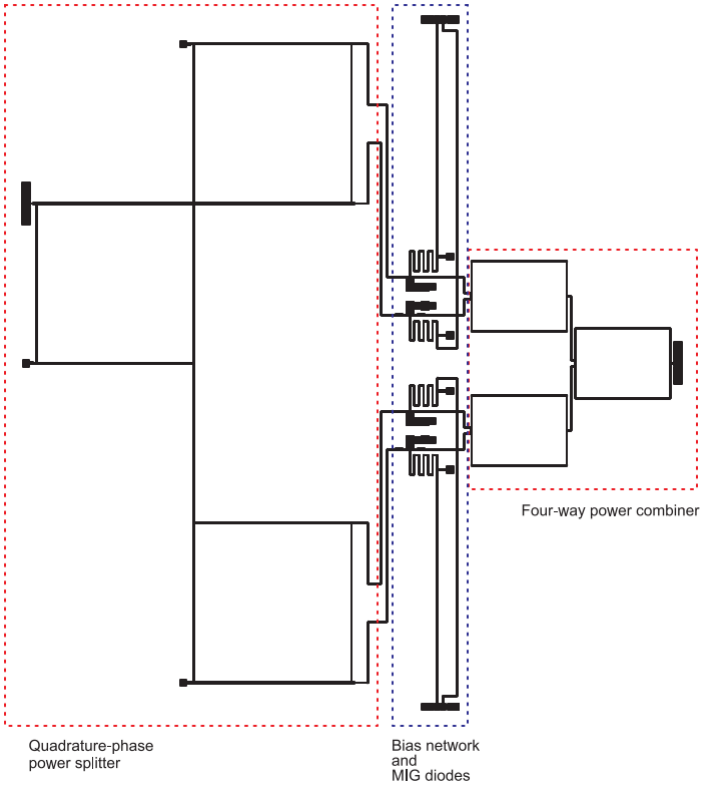


Figure 50 Layout of the designed 18 GHz transmitter employing graphene diodes

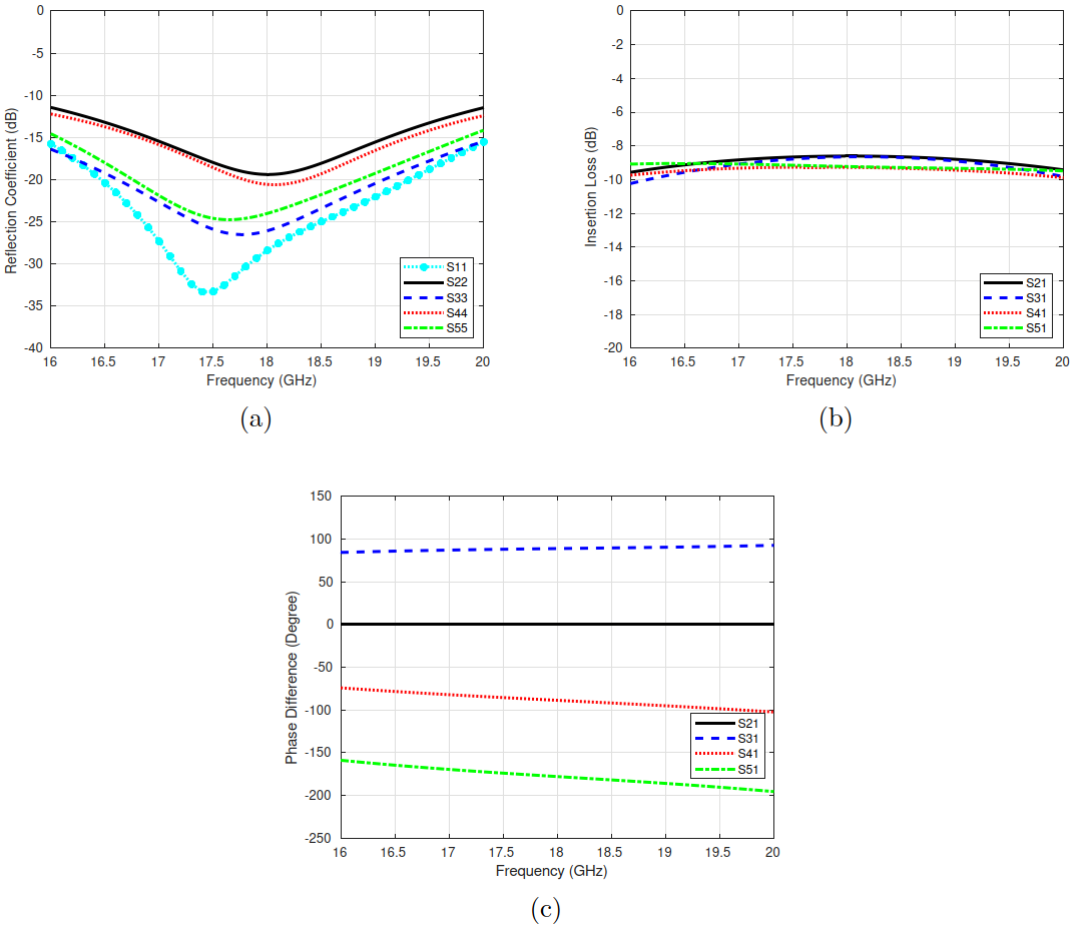


Figure 51 Simulated S-parameters of the power splitter operating at 18 GHz: (a) reflection coefficient, (b) insertion loss, and (c) phase difference

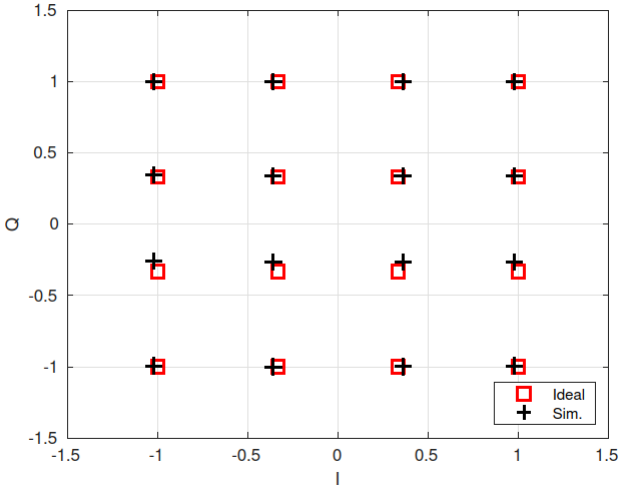


Figure 52 Simulated output constellation of the transmitter operating at 18 GHz

5 Cointegration of Graphene and TMDC Technology

Currently, there are two primary challenges in advancing RF systems based on 2D materials. Firstly, although graphene possesses high mobility and conductivity, its lack of an energy bandgap inherently limits its performance in transistors. This leads to low ON/OFF current ratios and limited current saturation in these devices, which restricts their application in digital and analogue circuits. Nonetheless, graphene-based diodes exhibit exceptional behaviour in high-frequency applications, leveraging the nonlinearity and high mobility of graphene to outperform other 2D materials. Secondly, transistors are a cornerstone of modern electronics. To address the limitations of graphene, MoS_2-based devices have emerged as a promising solution. However, the design of circuits utilizing TMD-based devices, particularly MoS_2-based transistors, has so far targeted lower frequencies. There has been a lack of reported technology processes suitable for monolithic microwave integrated circuits (MMICs). The existing designs mainly involve hybrid circuits where passive components like inductors, capacitors, and resistors are externally connected to the on-chip active device. Unfortunately, this approach constrains the achievable performance. Nonetheless, the reliance on external components has limited performance in terms of bandwidth and input power sensitivity.

Following the collaboration between AMO and RWTH, we address both challenges by introducing an MMIC process developed on an 8 µm-thick polyimide (PI) substrate. This process enables the creation of fully integrated flexible RF circuits. Notably, this work achieves the combination of two distinct CVD 2D material-based devices on a single chip: graphene-based diodes and MoS_2 FETs. Figure 53 illustrates the cross-section of this technology. The full back-end-of-line (BEOL) stack involves four metal layers. Metals M1 and M2 serve as the anode and cathode contacts for the metal-insulator-graphene (MIG) diode, with a 5 nm-thick sputtered TiO_2 layer acting as the insulator. Simultaneously, M1 functions as the bottom-gate for the MoS_2 transistor, while drain and source contacts are established using M3. The gate oxide consists of the thin TiO_2 layer along with a 40 nm Al_2O_3 layer. A 2 µm-thick top metal, M4, is utilized for implementing low-loss passives and interconnects. An 80 nm-thick encapsulation oxide follows the deposition of M4. The circuit also incorporates passive components, including spiral inductors formed using M1, metal-insulator-metal (MIM) capacitors constructed between M4 and M1, and thin-film resistors (TFR) made of a NiCr layer with a resistance of 65Ω/□. The active devices are characterized for their on-wafer DC performance, as depicted in Figure 54a and Figure 54b, showing results in line with the expectations. Moreover, additional characterization involving *S*-parameter analysis is conducted for the fabricated passive components, as shown in Figure 54c, demonstrating their typical frequency behaviour. This work has been published in Device Research Conference (DRC) 2023 under the title “Fully Integrated Flexible RF Detectors in MoS2 and Graphene based MMIC”.

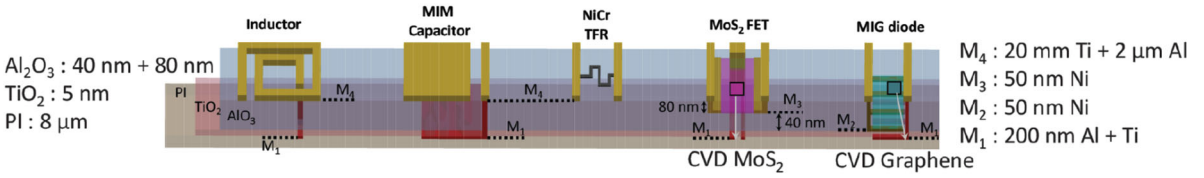


Figure 53 BEOL stack of the flexible MMIC technology. In order to be suitable for RF circuits it includes inductors, MIM capacitors and TFR resistors as passives, and MoS_2 FETs and graphene-diodes as active devices

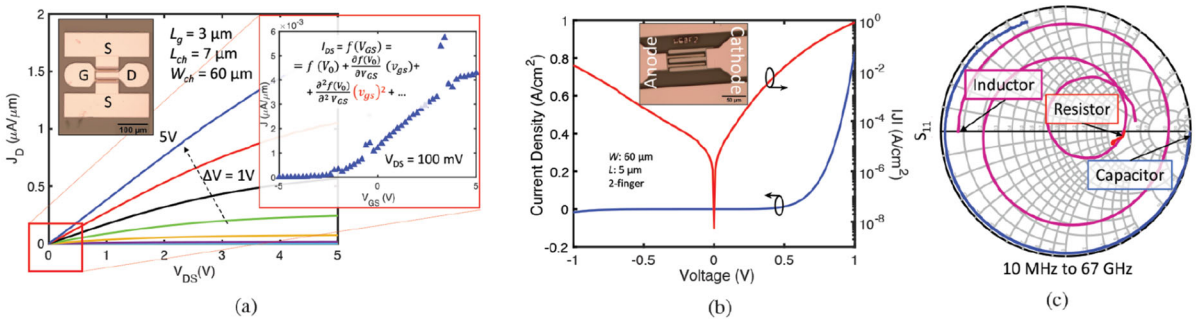


Figure 54 a) Measured output characteristics of the 2-finger MoS_2 FET. The micrograph of the device is included in the inset. Values L_g, L_{ch}, and W_{ch} are the gate length, channel length, and channel width, respectively. b) Characteristic curve of the MIG diode, which shows an asymmetry of around 200 at 1 V. Values W and L are the width and length per finger, respectively. The micrograph of the device is included in the inset. c) RF characterization by means of the return loss (S_{11}) of the on-chip passives.

6 Conclusions

This deliverable reports the progress and the results of the cointegration of antennae and graphene-based circuits. In the frame of the project, the integration of a metallic antenna together with graphene-based millimetre-wave frequency circuits could be successfully demonstrated, but not yet verified in measurements due to limitations of the available measurement setup.

Several high frequency transceiver concepts have been developed and successfully demonstrated in both commercial and experimental processes. All of the concepts can be applied with the necessary modifications to a further developed graphene MMIC process as well as to the frequency range in which graphene-based antennae show their advantages compared to canonical metal antennas.

This provides a platform for the future realisation of millimetre- and THz-wave wireless communication frontends for chip-to-chip applications.

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