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Architecting More than Moore – Wireless Plasticity for Massive Heterogeneous Computer Architectures †

D2.2: High performance graphene on wafer scale including encapsulation

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Executive Summary

In this deliverable, we describe how high performance graphene on wafer scale is realized in the WiPLASH project. We start from wafer-scale growth and transfer of graphene, which provides the material base for the fabrication. Since encapsulation is clearly targeted in this deliverable, we have introduced the two methods of encapsulation used within the WiPLASH project, which are based on the materials of aluminum oxide and SU-8. In the end, the quality control over wafer scale is summarized, with the definition of different parameters, as well as the performance on rigid substrate as well as flexible substrate, based on wafer scale. With this deliverable, we clearly demonstrate that high-performance wafer-scale graphene is accomplished in the WiPLASH project.

Abbreviations and Acronyms

ALD	Atomic Layer Deposition
Al_2O_3	Aluminium Oxide
AMICA	Advanced Microelectronic Center Aachen
CF_4	Carbon Tetrafluoride
CVD	Chemical Vapor Deposition
Cu	Copper
FWHM	Full Width at Half Maximum
GFET	Graphene Field-Effect Transistor
O_2	Oxygen
Pd	Palladium
PECVD	Plasma Enhanced Chemical Vapor Deposition
hBN	Hexagonal Boron-Nitride
HF	Hydrogen Fluoride
PI	Polyimide
PMMA	Poly(methyl methacrylate)
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
Si	Silicon
SiO_2	Silicon Dioxide
TLM	Transfer Length Method

The *WiPLASH* consortium is composed by:

UPC	Coordinator	Spain
IBM	Beneficiary	Switzerland
UNIBO	Beneficiary	Italy
EPFL	Beneficiary	Switzerland
AMO	Beneficiary	Germany
UoS	Beneficiary	Germany
RWTH	Beneficiary	Germany

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1 Introduction

The quality of graphene is critical for realizing graphene antennae. Among other material property parameters, the mobility as well as the Fermi level are of special importance. Figure 1 shows the dependency of the minimum mobility of a functional graphene antenna on the antenna length, for different Fermi energy levels. It is clearly demonstrated that the mobility and the Fermi energy can affect the design of the antenna significantly and, therefore, the reproducibility of these two parameters are the key figures leading to scalable applications.

In order to realize wafer-scale graphene suitable for antenna applications, we will describe the aspects of material synthesis, layer transfer, encapsulation and quality control, in the following chapters.

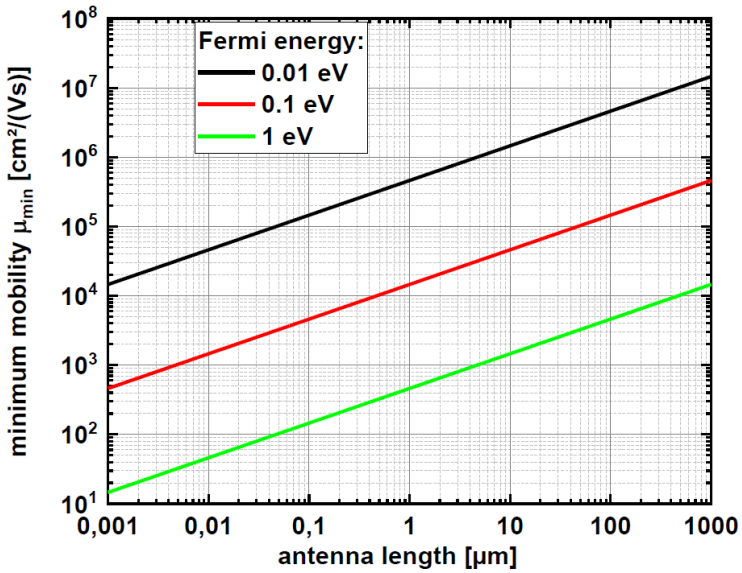


Figure 1. Minimum required mobility value for functional graphene antennae, as a function of the antenna length, for materials with different Fermi energy. [Süssmeier20]

2 Wafer-Scale Growth of Graphene

Graphene can be synthesized over wafer scale with a chemical vapor deposition (CVD) method. The process has to take place on a catalytic surface, which is usually copper (Cu), either in a form of Cu foil or Cu deposited on substrate (for example Cu grown on sapphire). Due to the polycrystalline nature of the Cu foil, the resulting graphene is also polycrystalline. On the contrary, Cu deposited on substrate can be already single crystalline (for example Cu111), so the resulting graphene can be of very high quality in this case.

2.1 Growth Tool

The partner AMO has access to a plasma enhanced CVD (PECVD) tool located in the cleanroom of the Advanced Microelectronic Center Aachen (AMICA), as shown in Figure 2, which can be utilized for the growth of graphene. This PECVD tool is able to be loaded with wafers of the size of up to 200 mm. The highest temperature is 1200 °C, and the maximum pressure of the chamber can reach 4 Torr.

Figure 2. PECVD tool for graphene growth, located in the cleanroom of AMICA.

2.2 Process Flow

The established process at AMO is based on Cu foil (size 150 mm x 150 mm) with a process of annealing of the Cu foil, growth, and cooling down. The whole process with the gas inlet is shown in Figure 3. As demonstrated, argon and hydrogen is used during the phase of annealing. Methane is used as a carbon source during the growth. In the cooling phase, argon is applied to provide an inert atmosphere.

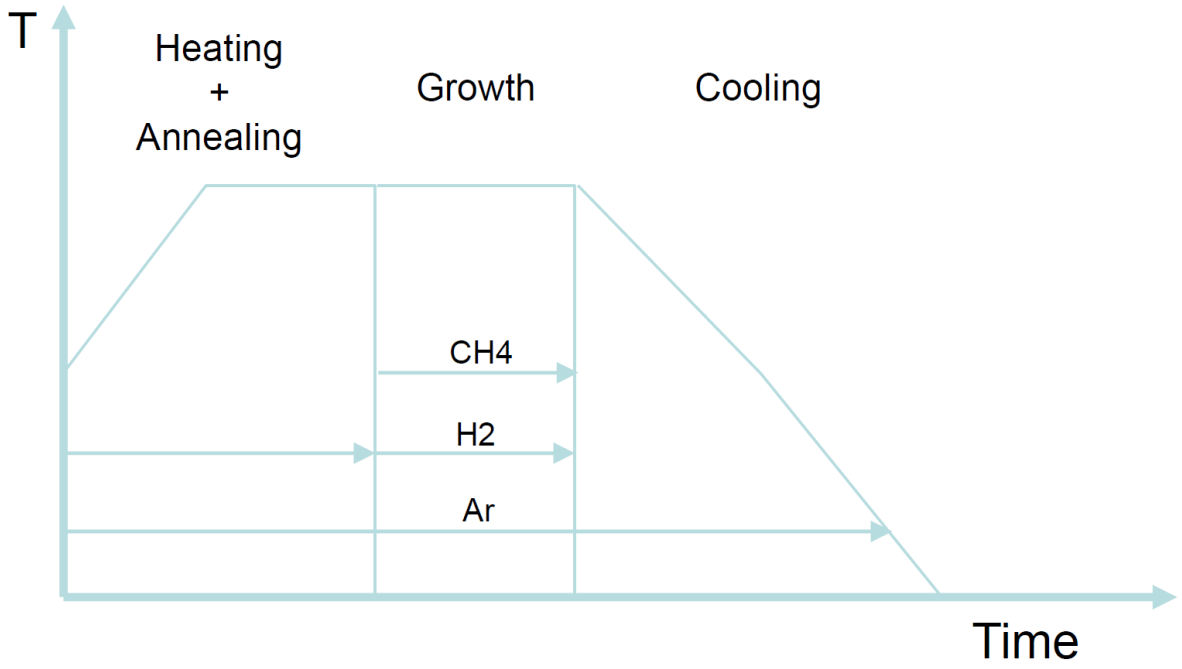
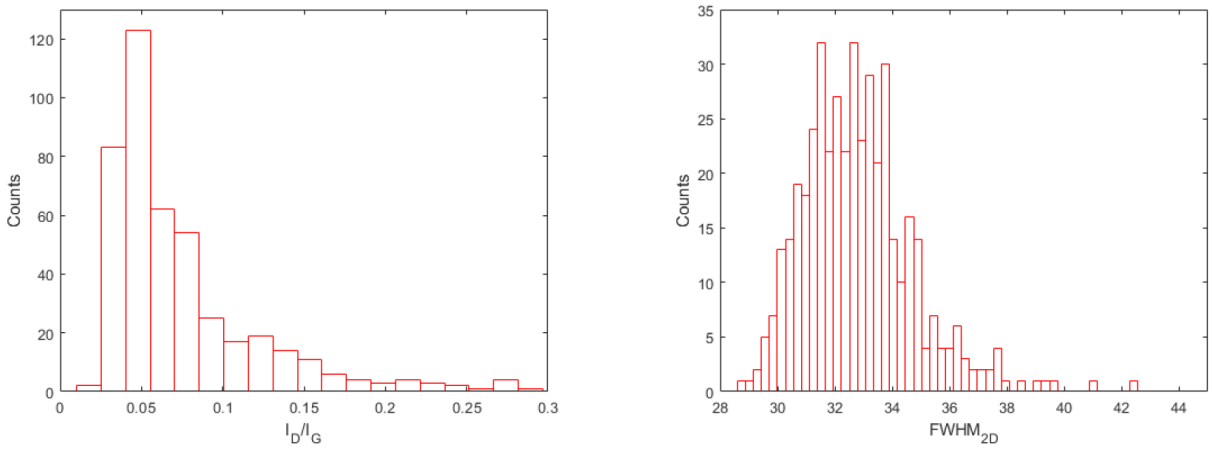


Figure 3. The complete growth process of graphene in a PECVD tool.

2.3 Raman Characterization

The resulting graphene film can be characterized with Raman in order to identify the quality, either directly on the underlying Cu substrate (this requires a special wavelength) or after transfer onto a target substrate (this will be described in the next chapter). The practice at AMO is to characterize the film after the transfer process to a silicon/silicon-dioxide (Si/SiO_2) wafer, due to a limitation on the wavelength in the available Raman system. In Figure 4, histograms of the intensity ratio between D- and G-peak (I_D/I_G), as well the full width at the half maximum of the 2D-peak ($FWHM_{2D}$) has been shown for a growth on a Cu foil of 150 mm x 150 mm. It is clearly demonstrated with low D-peak intensity (I_D/I_G ~ 0.05), which suggests very low defect density of graphene. Moreover, the low $FWHM_{2D}$ (32~34 cm^{-1}) indicates the nature of monolayer graphene, also that there is a good interface between graphene and the substrate [Banszerus17].



(a) (b)

Figure 4. Histogram of Raman parameters for graphene grown over wafer scale. (a) I_D/I_G and (b) $FWHM_{2D}$.

3 Wafer-Scale Transfer of Graphene

As already described in the previous chapter, graphene is grown on a catalytic substrate such as Cu, so a process to transfer graphene onto a target substrate is required to be realized over wafer scale.

3.1 Process Flow

In WiPLASH we use a poly(methyl methacrylate) (PMMA) based process to realize wafer-scale graphene transfer. The basic process flow is illustrated in Figure 5. First, the graphene grown on Cu is coated with PMMA, and then the Cu foil is etched in solution. The PMMA/Graphene stack is transferred to the target substrate, followed by removal of the PMMA. This process has been demonstrated successfully on smaller scale worldwide but to scale this process up to entire wafers is still challenging. The delamination of the graphene after the transfer and the PMMA residue on graphene are the main issues.

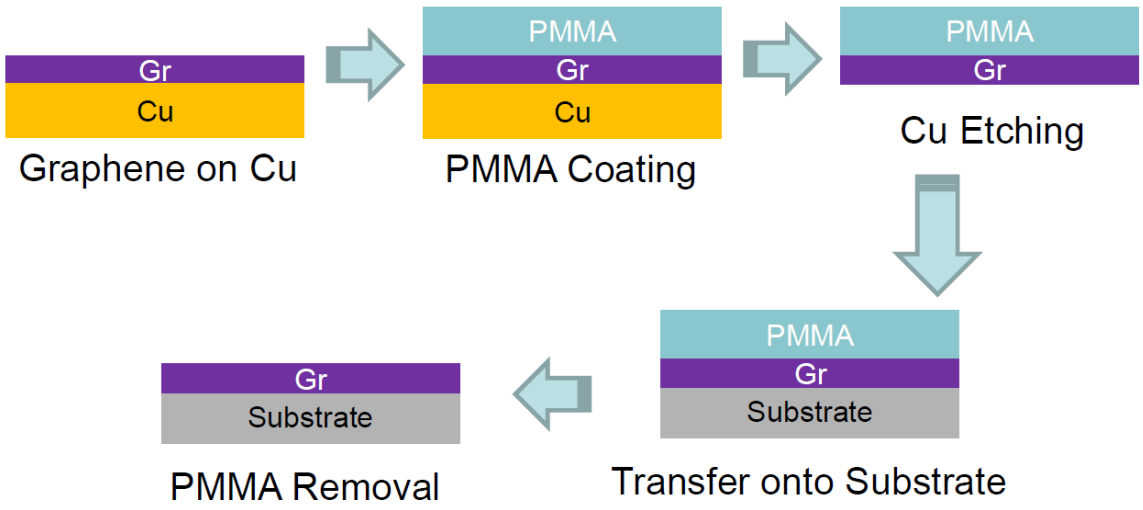


Figure 5. Process of graphene transferred, with PMMA as a supporting layer.

3.2 Results

At AMO, this transfer process was successfully scaled up to wafers of a size of 150 mm . A photo taken with the optical microscope of such a 150-mm wafer after graphene transfer is shown in Figure 6. Images taken with the scanning electron microscope (SEM) are presented in Figure 7. The result does not present a problem of graphene delamination, although some holes are visible. Grain boundaries and bilayer islands are also visible in the images, but this is intrinsically related to the graphene growth process based on PECVD.

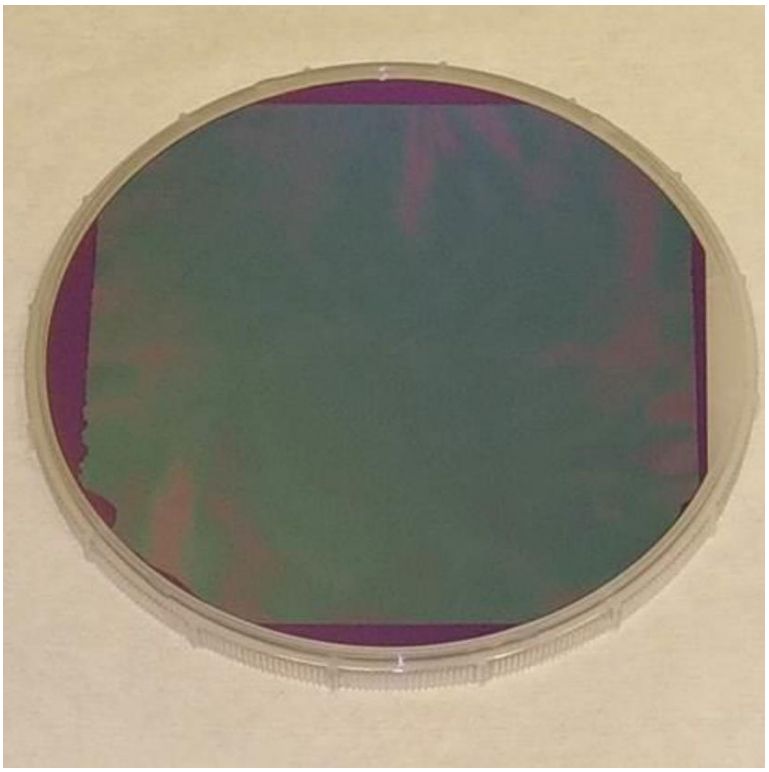
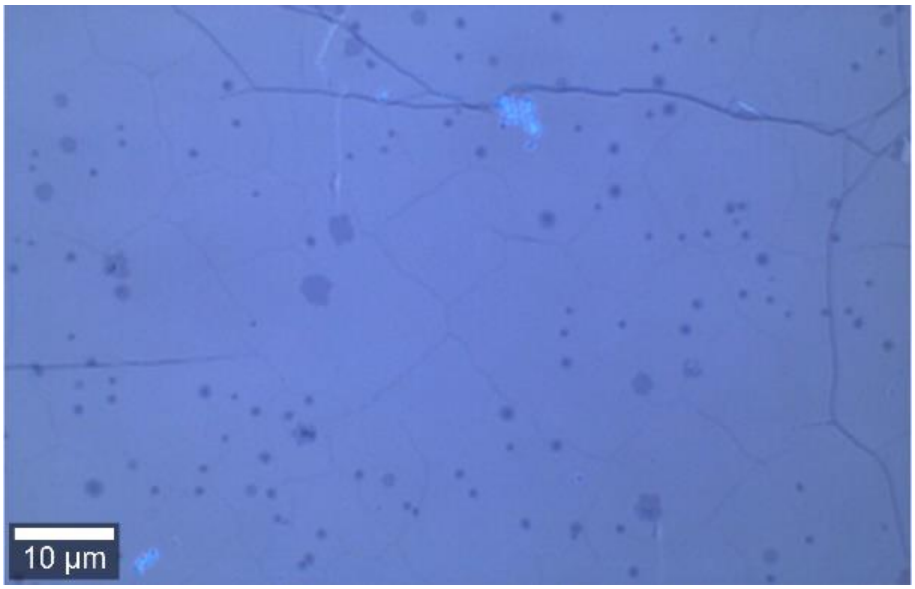


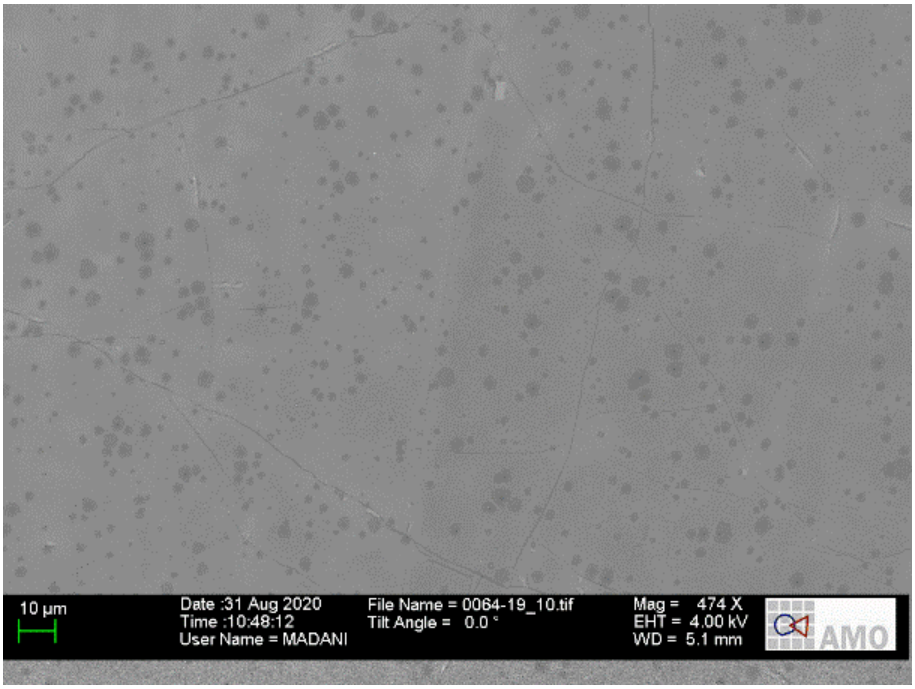
Figure 6. Graphene transferred onto Si/SiO_2 substrate, with PMMA still on top.

Nevertheless, we can conclude that the morphology of graphene shown in Figure 7 already meets the requirement of the application in WiPLASH, since we are focusing here on demonstrations of the feasibility and capabilities instead of product development. In the end, if a production is foreseen for graphene-based application, an improved process, *e.g.* growth on Cu111 substrate, is needed. This is still in development in the graphene community, but not a focus of WiPLASH.

The resulting film shown in Figure 7 has been also characterized with Raman spectroscopy and the result is shown in Figure 4.



(a)



(b)

Figure 7. (a) Optical microscope image and (b) SEM image of graphene transferred onto Si/SiO_2 substrate.

4 Encapsulation of Graphene

The encapsulation of graphene is generally realised via two approaches at AMO: (1) atomic layer deposition (ALD) of aluminium oxide (Al_2O_3) and via etching; (2) A epoxy-based negative photoresist SU-8 coating and patterning. Although the Al_2O_3 approach requires higher process complexity, it is a standard encapsulation solution and, therefore, facilitates the compatibility with various applications. Conversely, the SU-8 approach offers simplified processing, but with slightly limited application compatibility.

4.1 Al_2O_3 Encapsulation

Al_2O_3 of 60-80 nm grown by a thermal-based ALD process is employed as encapsulation layer. ALD-grown Al_2O_3 needs to be etched for opening vias on the encapsulation layers to allow electrical contacting. The existing wet etching method using buffered hydrogen fluoride (HF), for example, is not ideal for scaling-up due to lack of reproducibility and uniformity of the etching profile on wafer scale. Therefore, a more reproducible and controllable dry etching method using reactive ion etching (RIE) is more favourable. Among different RIE etchants evaluated, the combination of carbon tetrafluoride (CF_4) and oxygen (O_2) was found to deliver residue-free, uniform, and controllable (22 nm/min) etching results and, therefore, was employed for the RIE etching of Al_2O_3 for via opening.

A representative optical image of via areas is shown in Figure 8.

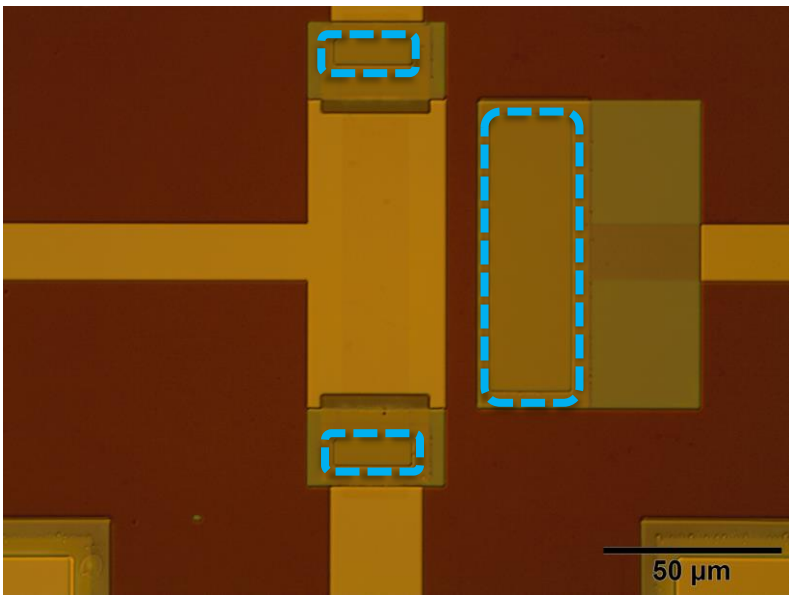


Figure 8. Optical microscope image of a typical GFET device, with vias (dashed areas) opened by RIE processing on contact pads.

4.2 SU-8 Encapsulation

Another feasible encapsulation solution is to use a protective SU-8 layer, combined with lithographic patterning of via areas for electrical contacting. The SU-8 protective

layer is spin-coated and then patterned for via opening via a negative photo-lithography process, followed by hard-baking to achieve desirable mechanical stability required as encapsulation layer.

An SU-8 encapsulated device with via opening can be seen in the following optical image (Figure 9).

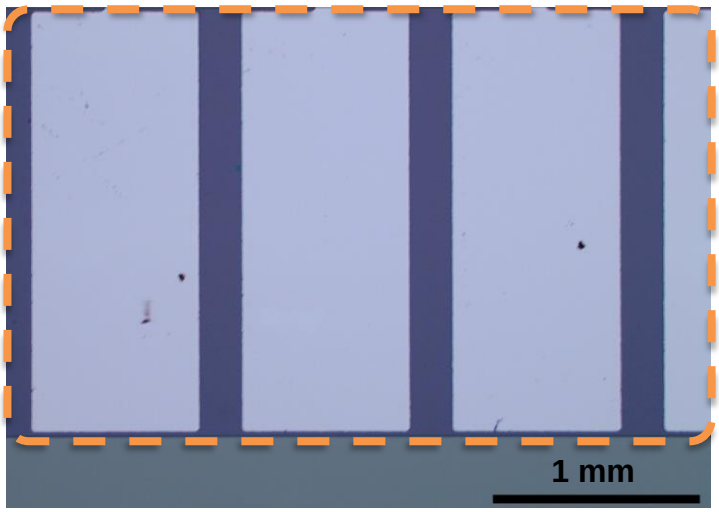


Figure 9. Optical microscope image of SU-8 encapsulation and via opening of contact pads (dashed area).

5 Quality Control on Wafers

To ensure high yield and reproducibility, a suitable monitoring protocol was developed for in-line inspection and quality control to ensure qualification of graphene during and after each processing run. The gated transfer length method (TLM) was employed to determine contact resistance, mobility, and Dirac point. The gate-dependent contact resistance between graphene and an applied electrode as well as the sheet resistance by the formation of a set of electrodes are determined. Moreover, measurement of the total resistance between the electrodes are carried out in this regard. A typical TLM pattern consists of uniform graphene devices with varying channel lengths (L_1, L_2, …) and identical channel widths (W) designed and implemented by lithography, as shown in Figure 10(a).

Transfer characteristics of gated TLM channels were measured with three probes connected to the source, drain, and gate terminals, respectively. The gate-voltage (V_g) dependent total resistance (R_{total}) of each channel was measured by applying a voltage, e.g. V_d= 100 mV, across the contacts and measuring the resulting drain current, I_d. The gate sweep range needs to be selected so that the carrier concentration level of ± 5e12 cm^{-2} is reached, with gate compliance of 100 nA. The gate-voltage steps should be set in such a way that each single $I_d - V_g$ sweep contains no fewer than 100 data points. The sweep is measured at least once in the back- and one in the forward direction to extract the hysteresis.

5.1 Contact resistance

The total resistance, R, consisting of the channel resistance of the graphene-sheet and the contact resistance of the graphene/metal junction, can be expressed as $R(L) = R_{sheet} L/W + 2R_c/W$, where R_{sheet} is the sheet resistance of graphene, R_c/W is the contact resistance normalized to the contact width W, and L is the channel length. The total resistance R of devices with different channel length L_1, L_2, L_3 and L_4 can be plotted as a function of channel length (L), as shown in Figure 10(b). It should be noted that the data points from different devices here should be with the same doping level. By linear fitting R(L), R_{sheet} and R_c can be extracted from the slope and intercept, respectively. By fitting R(L) for different doping level, i.e. gate voltage, we can also get gate-dependent R_{sheet} and R_c.

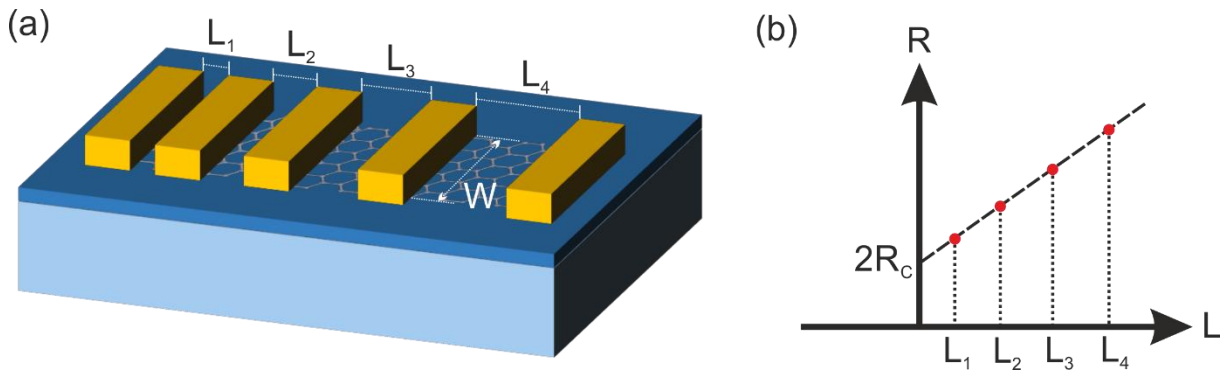


Figure 10. TLM to extract the contact resistance between metal and graphene. (a) The device series. (b) The linear fitting of the resistance.

As described in Deliverable D2.1, bottom contacts with metal palladium or edge contacts with metal nickel are used for wafer-scale fabrication of the graphene antenna.

5.2 Mobility and Fermi Energy

Mobility can be extracted from the aforementioned gate-dependent sheet resistance, $R_{sh,}$ according to the field-effect mobility model. Using the gate-voltage-dependent transconductance of the graphene field-effect transistors (GFETs), the field-effect mobility, μ, was calculated as $\mu = g_m L/(WV_dC_g)$, where the transconductance is given by $g_m = \frac{\partial G_{sh}}{\partial(V_g - V_{cnp})}$, with $G_{sh} = 1/R_{sh}$; L and W are the graphene channel length and width; V_d is the drain voltage, $C_g = \varepsilon\varepsilon_0/t_{ox}$ is the gate capacitance with t_{ox} defining the thickness of the gate dielectric.

5.3 Performance on Wafer Scale

Please note, this Section 5.3 has been shown in Deliverable D2.1 and here we describe it again in order to ensure the completeness of this deliverable.

The palladium (Pd) bottom-contacted devices have been scaled up to 200 mm Si wafers. 90-nm thick SiO_2 is used as gate dielectric. The statistics of four-point field-effect mobility for encapsulated devices is shown in Figure 11. The mobility has a relatively narrow distribution between 3000 and 5000 cm^2/Vs, but there is still a long tail towards lower mobilities.

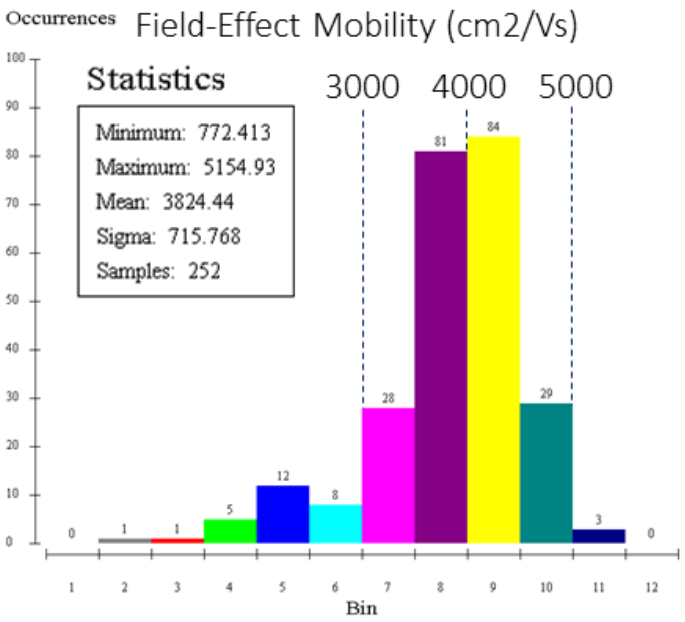


Figure 11. The histogram of the field-effect mobility of encapsulated devices with Pd bottom contact, based on 200-mm Si substrates.

Besides, we have explored the performance of graphene on polyimide (PI), which is a flexible substrate with a thickness of about 8 µm. The developed edge contact process is scalable to wafer sizes up to 150 mm. We have fabricated top-gated field-effect device, so the devices are encapsulated by the top-gate dielectric. The 4-point van der Pauw method was used to extract the field-effect mobility, and the statistics are shown in Figure 12. The extracted average sheet resistance at the Dirac point is about 5.8 kΩ, whereas the average mobility is about 3230 cm^2/Vs.

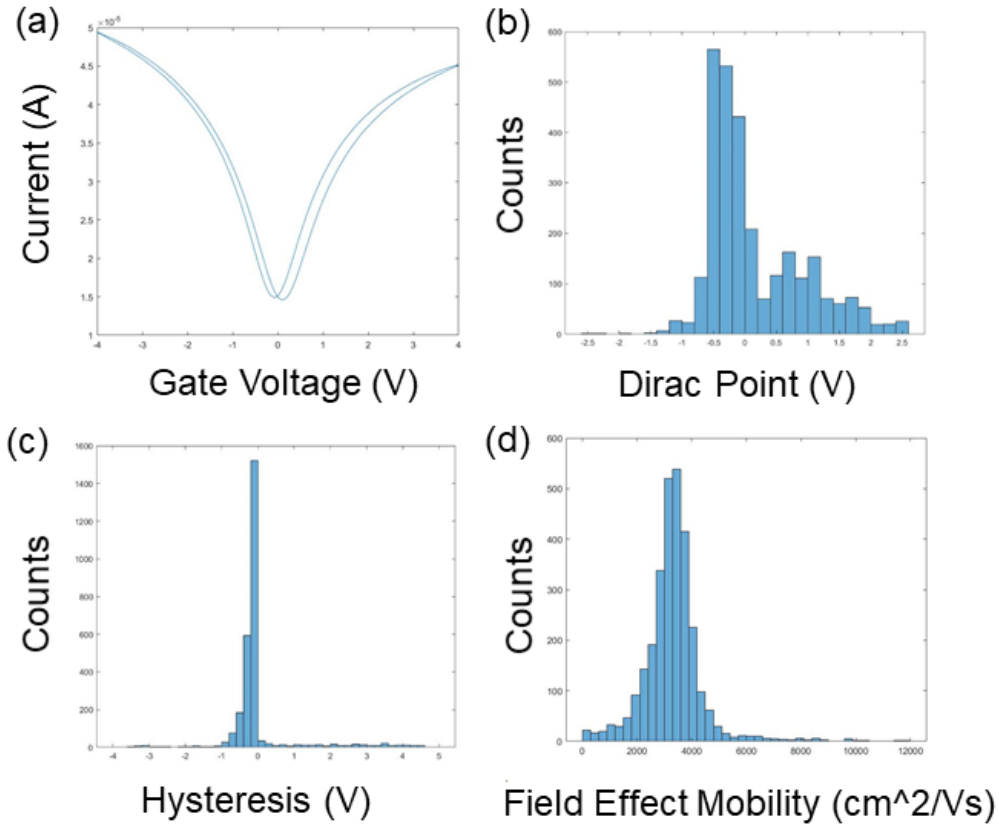


Figure 12. The performance of top-gated devices on flexible PI substrate, with wafer scalable process. (a) Transfer characteristics of a single device. (b) Histogram of the position of the Dirac point. (c) Histogram of the hysteresis. (d) Histogram of the field-effect mobility.

All these scalable processes with different substrate as well as different metal-graphene contact schemes enable us for wafer-scale fabrication of graphene antennae.

6 Discussion

We have shown in this deliverable that the complete process flow for wafer-scale graphene production and fabrication is available at AMO. The final target in WiPLASH is to use such graphene for antenna fabrication. Therefore it is necessary that we analyze the feasibility of such graphene for antenna fabrication. **In principle, we can conclude that the wafer-scale graphene presented here meets the basic requirement for graphene antenna.** Below are the detailed analysis and discussion.

We have reported in deliverable D2.1 that the Fermi energy of the graphene at AMO is about 0.3 eV. As plotted in Figure 1, the minimum mobility requirement for graphene antenna with length of 1 µm is about 5000 cm^2/Vs. If we reduce the length of antenna further to 500 nm, the minimum requirement is then also reduced to 3000 to 4000 cm^2/Vs. The mobility range 3000 to 5000 cm^2/Vs is already what we have at AMO. However, back to the dimension, it is not an easy task at this moment to realize wafer-scale fabrication down to sub-micron size. The most mature technology utilized at AMO for graphene processing is contact lithography, which limits the resolution to 5 µm. Indeed an i-line stepper is available at AMO, with resolution down to 400 nm, but the process base on this tool is still an on-going development.

In the end, the limitation on the dimension would then lead to higher requirement on the mobility. Materials such as hexagonal boron-nitride (hBN) become necessary in order to preserve the high mobility of graphene on substrate. [Dean10] However, the maturity of hBN is not yet ready to offer high quality over large scale. It is feasible to have high quality material for a dimension of e.g. 40 µm, but this is far away from wafer scale. Large-scale CVD hBN material is commercially available but the advantage brought by this material is not clear, since it does not really boost the mobility of graphene.

To sum up, future work (not only limited to WiPLASH) includes mainly: (1) Further development of graphene process based on i-line stepper in order to achieve smaller dimension; (2) Keep track on the development of hBN material. Besides this, we can use the technology and material we have to demonstrate the basic function of the graphene antenna, for example, to combine e-beam lithography (which is not a scalable process but can achieve small dimension) and the CVD graphene we have presented in this deliverable.

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