Horizon 2020 Program (2014-2020)

FET-Open Novel ideas for radically new technologies

FETOPEN-01-2018-2019-2020

Architecting More than Moore – Wireless Plasticity for Massive Heterogeneous Computer Architectures †

D2.1: First co-integration of graphene antennas with full custom SiGe transceivers

Contractual Date of Delivery	31/03/2021
Actual Date of Delivery	29/03/2021
Deliverable Security Class	Public
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† This project is supported by the European Commission under the Horizon 2020 Program with Grant agreement no: 863337

Document Revisions & Quality Assurance

Deliverable Number	D2.1
Deliverable Responsible	AMO
Work Package	WP2
Main Editor	Zhenxing Wang (AMO)

Internal Reviewers

1. Peter Haring Bolívar (UoS)
2. Alexandre Levisse (EPFL)

Revisions

Version	Date	By	Overview
1.0	1/3/2021	Zhenxing Wang (AMO)	First draft with structures
1.1	15/3/2021	Zhenxing Wang (AMO), Kun-Ta Wang (AMO), Elana Pereira de Santana (UoS), Mohamed Elsayed (RWTH)	Input from partners
1.2	19/3/2021	Zhenxing Wang (AMO), Mohamed Elsayed (RWTH)	Input from partners
2.0	19/3/2021	Zhenxing Wang (AMO)	First complete version
2.1	26/3/2021	Peter Haring Bolívar (UoS), Alexandre Levisse (EPFL), Zhenxing Wang (AMO)	Revised version with the input from internal reviewer
3.0	29/3/2021	Zhenxing Wang (AMO)	Final version

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Executive Summary

In this deliverable, we have described how to realize a co-integration of graphene antennas with full-customized SiGe technology. All the required building blocks are discussed in details, and the integration route is provided.

In order to enable graphene technology integrate on the conventional SiGe platform, the scalability of the graphene process is the first question that needs to be addressed. We have developed a standard process at AMO to make ohmic electrical contact to graphene, either on rigid Si/SiO_2 substrate or on flexible polyimide substrate. This process is scalable up to 200 mm wafer and in the meantime compatible with the fabrication flow for graphene antenna. Antennas on different substrates as well as with various electrode materials have been fabricated and characterized, in order to identify the optimized combination for THz graphene antenna, that is able to deliver the best performance. Through substrate via is crucial for the demanding hetero-integration. Regarding this we have provided solutions for both flexible substrate and rigid substrate, the so called through glass via in the case for rigid substrate. Furthermore, the design for the customized SiGe circuits has been presented, with different functions such as amplifiers, mixers, ring oscillators, and so on. In the end, the route for co-integration has been demonstrated, based on all the building blocks that has been successfully shown in this deliverable. The results presented in the deliverable include all key components necessary for the nano-integration technology demonstration at this early stage of the project, although the fully functional demonstration is planned at a later stage, related to deliverable D2.3 Full transceiver / antenna system with high performance ready for measurements, in project month 30.

Abbreviations and Acronyms

Al	Aluminium
Au	Gold
DSB	Double-Side Band
GaAs	Gallium Arsenide
HR-Si	High Resistivity Silicon
HR-Si+	Si+ Ion Implanted High Resistivity Silicon
IC	Integrated Circuit
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuit
Ni	Nickel
Pd	Palladium
PI	Polyimide
RF	Radio Frequency
Si	Silicon
SiGe	Silicon-Germanium
SiO_2	Silicon Dioxide
SOLT	Short-Open-Load-Through
SPP	Surface Plasmon Polariton
TDS	Time-Domain Spectroscopy
TGV	Through Glass Via
THz	Terehertz

The *WiPLASH* consortium is composed by:

UPC	Coordinator	Spain
IBM	Beneficiary	Switzerland
UNIBO	Beneficiary	Italy
EPFL	Beneficiary	Switzerland
AMO	Beneficiary	Germany
UoS	Beneficiary	Germany
RWTH	Beneficiary	Germany

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1 Process Development for Scalable Graphene Antenna

We have developed different process flow, which can be potentially used for graphene antenna fabrication. Depending on the required performance, various metal-graphene contact schemes as well as different substrates are considered. In this section, we will start with the standard process at AMO, including two different contact schemes. Afterwards we discuss about the scalability of this process on different substrates.

1.1 Standard Process

We have developed standard graphene technology at AMO, which can be used for graphene antenna fabrication. Mainly there are two different contact schemes, between metal electrode and graphene, i.e. bottom contact and side (or edge) contact, as shown in Figure 1.

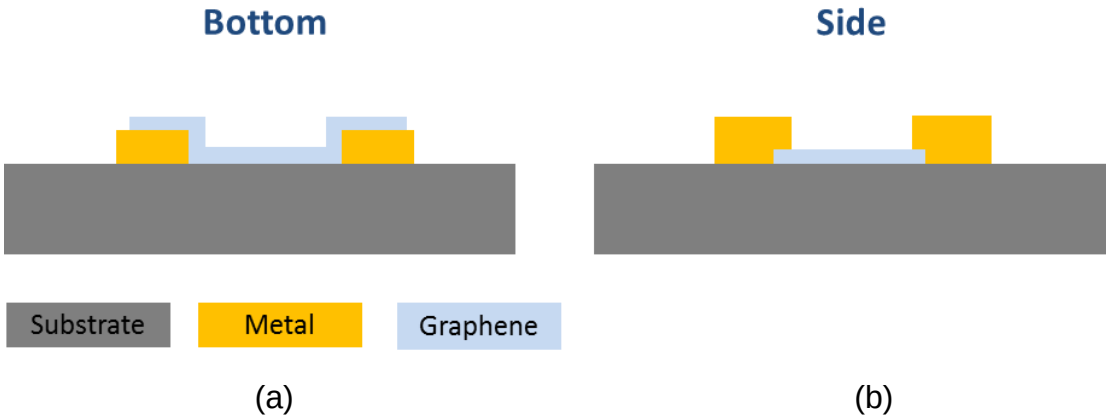


Figure 1. The standard process at AMO with two different metal-graphene contact schemes.

Bottom contact is realized with metal palladium (Pd) and the thickness of the metal should be small enough (normally <50 nm) to make sure that graphene does not break at the edge of the metal eletrodes. The process starts with metal contact deposition, followed by graphene transfer and patterning.

The mobility for the bottom-contacted devices on silicon (Si) / silicon dioxide (SiO_2) substrate is in the range of 3000~5000 cm^2/Vs after encapsulation (four-point field-effect mobility, maximum value at highest transconductance point); before encapsulation it is 2000~3000 cm^2/Vs. The carrier concentration at $V_g = 0$ is in the range of $11 \cdot 10^{12}$~$17 \cdot 10^{12}$ cm^{-2} (variation due to the hysteresis), corresponding to E_F of 0.38~0.48 eV. The contact resistance is higher than side contact, but this process is reproducible and with high yield.

Side contact is realized with metal nickel (Ni) [Shaygan2017]. A layer, e.g. aluminium (Al) deposited on top of Ni is possible to increase the conductivity of the metal. This process starts with graphene transfer, followed by metal contact deposition, and graphene patterning in the end.

The mobility for the edge-contacted devices on Si/SiO_2 substrate is similar to that of bottom-contacted devices. The carrier concentration at $V_g = 0$ is in the range of

$6 \cdot 10^{12}$~$10 \cdot 10^{12}$ cm^{-2} (variation due to the hysteresis), corresponding E_F of 0.29~0.37 eV. The contact resistance is well below 1 kΩ·µm.

1.2 Scalability of the Process

The Pd bottom-contacted devices have been scaled up to 200 mm Si wafer. 90 nm SiO_2 is used as gate dielectric. The statistic of four-point field-effect mobility for encapsulated devices is shown in Figure 2 with a statistics. The mobility has a relatively narrow distribution between 3000 and 5000 cm^2/Vs, but still there is a long tail at lower mobility side.

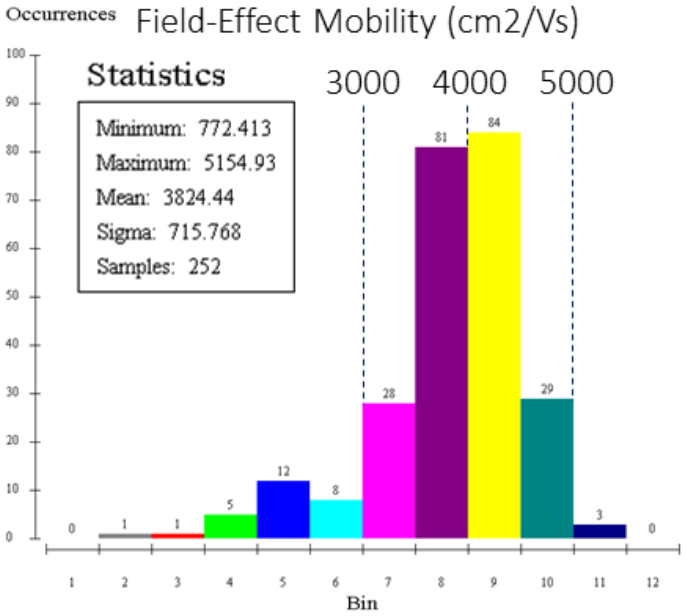


Figure 2. The histogram of the field-effect mobility of encapsulated devices with Pd bottom contact, based on 200 mm Si substrate.

Besides, we have explored the performance of graphene on polyimide (PI), which is a flexible substrate with thickness of about 8 µm. This edge contact process is scalable up to 150 mm wafer size. We have fabricated top-gated field-effect device, so the devices are encapsulated by the top-gate dielectric. 4-point van der Pauw method was used to extract the field-effect mobility, and the statistics are shown in Figure 3. Average sheet resistance at Dirac point is about 5.8 kΩ. Average Mobility is about 3230 cm^2/Vs.

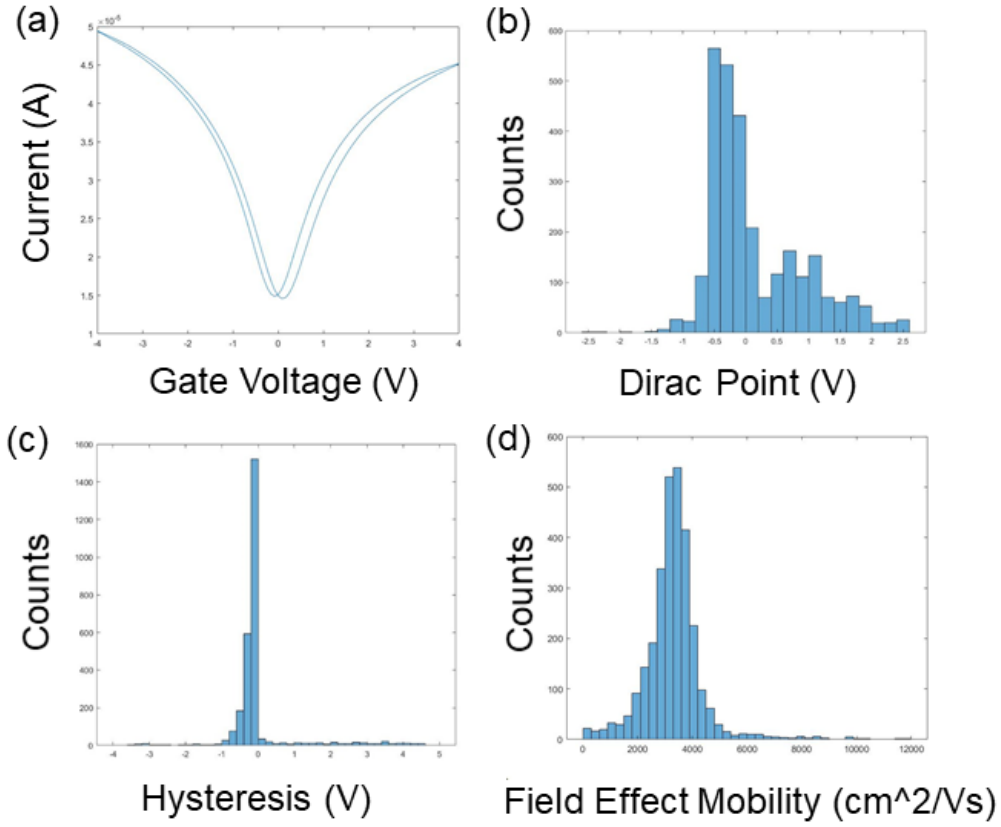


Figure 3. The performance of top-gated devices on flexible PI substrate, with wafer scalable process. (a) Transfer characteristics of a single device. (b) Histogram of the position of the Dirac point. (c) Histogram of the hysteresis. (d) Histogram of the field-effect mobility.

All these scalable process with different substrate as well as different metal-graphene contact schemes enable us for the wafer scale fabrication of graphene antenna, which is one of the main objective of WiPLASH.

2 Design and Fabrication of Graphene Antenna

Graphene antenna has been designed based on the material properties based on the standard and scalable process available at AMO.

2.1 Design of Graphene Antenna

The chosen design of a first graphene antenna for integration with silicon-germanium (SiGe) transceivers is a dipole antenna, on which an excitation between the antenna arms allows radiation to the free-space.

In case of a metal antenna, the resonating frequency is defined by the antenna length and materials used following the equation below [Tani1997, Silver1984]:

$$f_R = \frac{c_0}{2L\sqrt{\frac{\varepsilon_1 + \varepsilon_2}{2}}}$$

Here f_R is the resonant frequency, L the antenna length, ε_1 and ε_2 the permittivities of the substrate and superstrate.

In case of a graphene antenna, the resonance frequency is not only dependent on its dimensions, substrate and superstrate material, but also on its Fermi level, following the equation below, after combining the surface plasmon polariton (SPP) dispersion relation [Jablan2009] with the antenna resonance condition [Llatser2012, Süssmeier2020]:

$$f_R = \sqrt{\frac{e^2 E_F}{4\pi^2 \hbar^2 \varepsilon_0 (\varepsilon_1 + \varepsilon_2)}} \cdot \frac{1}{\sqrt{L}}$$

Here E_F is the Fermi energy level, e is the electrical charge, ε_0 is the vacuum permittivity and $\hbar$ is the reduced Planck's constant.

The fact that the resonance frequency of the graphene antenna is also dependent on its Fermi level, allows one to tune it by only changing the Fermi level, what can be done chemically or electrically [Llaster2012, Abdal2017].

By comparing the dimensions of a metal antenna and a graphene antenna resonating at the same frequency (Figure 4), the use of graphene allows the reduction of the antenna size by orders of magnitude. A reduction that increases more with lower graphene Fermi levels.

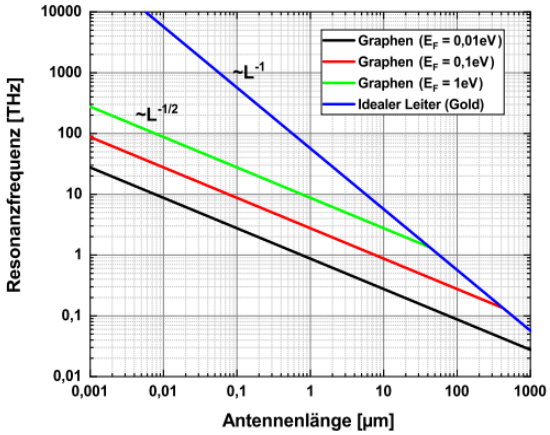


Figure 4. Resonance frequency vs. antenna length. [Süssmeier2020]

However, taking into account the relation between the relaxation time and mobility of charges in graphene, the low Fermi energy that would be advantageous for size reduction of the antenna leads to a need of a much higher mobility value, as can be seen in Figure 5, that with the manufacturing processes used nowadays are challenging to achieve.

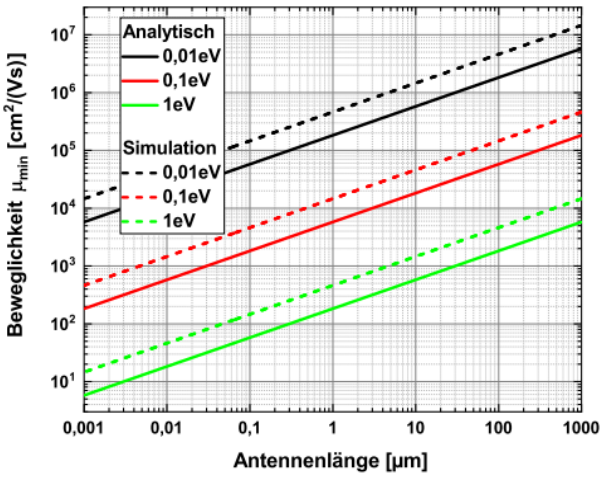


Figure 5. Mobility vs. antenna length. [Süssmeier2020]

In this case, a compromise between antenna size reduction, Fermi level and mobility must take place [Süssmeier2017].

For our design shown in Figure 6, the antenna length is L = 50 µm and 40 µm in a H shape. The gap between the antenna arms is g = 5 µm and the width of the antenna arms is W = 5µm.

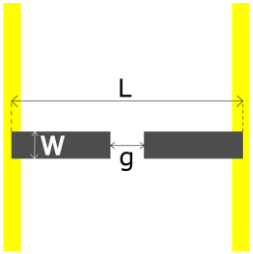


Figure 6. Current design of the graphene antenna.

Typical photoconductive antennas of this kind are fabricated using gold (Au) on top of gallium arsenide (GaAs) substrates. For integration of the graphene antennas with the SiGe technology, we propose to change the substrate to a high-resistivity silicon substrate. Besides, for a compatible manufacturing process with AMO, Pd metal is used instead of Au.

The H-dipole antenna is one of the most practical way to prove the terahertz (THz) radiation of a graphene antenna by means of optical excitation on its gap. Different antenna designs excited electrically are still being studied by UoS for integration with the SiGe technology.

The mix-match compatibility between photolithography and e-beam lithography has been considered, in case that we would need to go for smaller dimension, which is beyond the resolution limit of photolithography. Figure 7 shows our basic design of the antenna, both for metal antenna as a reference device and graphene antenna Figure 7a is metal antenna structure, with this design we fabricate antenna with different combinations of substrate and metal to identify which one has optimized performance and compatibility with process flow at AMO. Figure 7b shows the final design with graphene antenna.

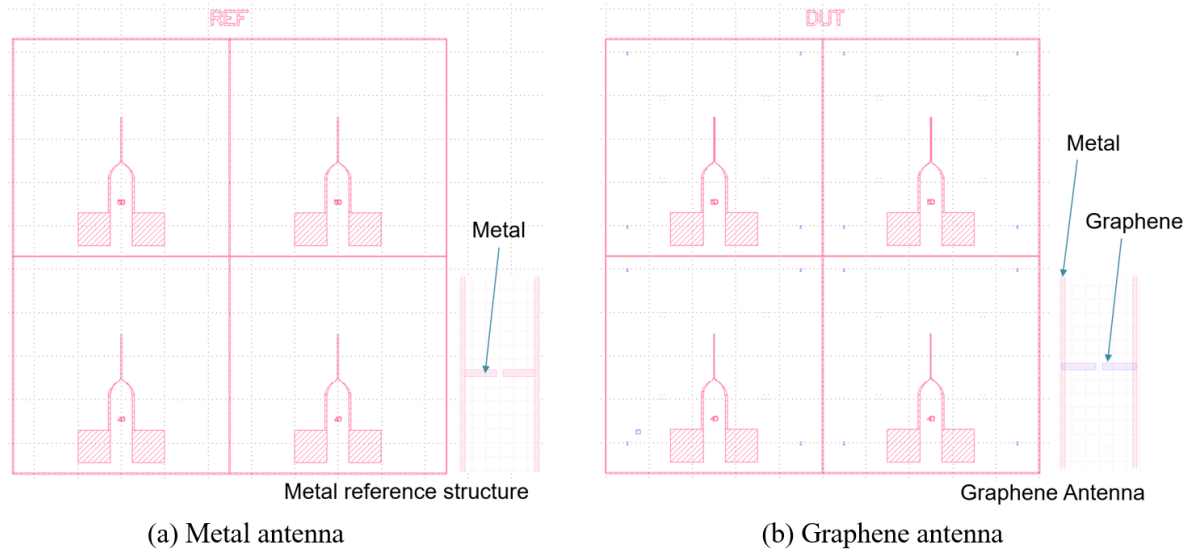


Figure 7. Layout design for antennas. (a) Metal antenna structure and (b) Graphene antenna structure.

2.2 Fabrication of Graphene Antenna

High reproducibility and yield is highly demanded by WiPLASH since in the end the process should be scalable up to wafer size. Therefore we have decided to start with the bottom contact. However, the substrate has to be adapted to semiconductor substrates. The process flow has been summarized below:

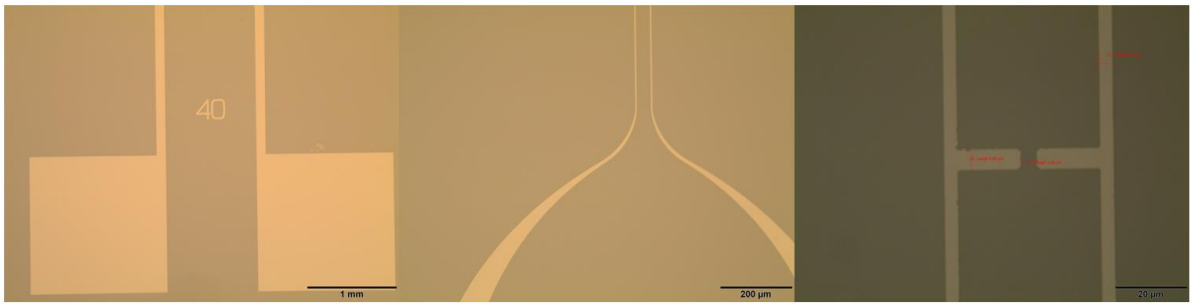
- Step 1: Deposition of metal electrodes by a lift-off process, photolithography will be used.
- Step 2: Graphene transfer

- Step 3: Depending on the dimension, either photolithography or e-beam lithography, together with oxygen plasma etching, will be used to pattern graphene. Mask mix-match possible.

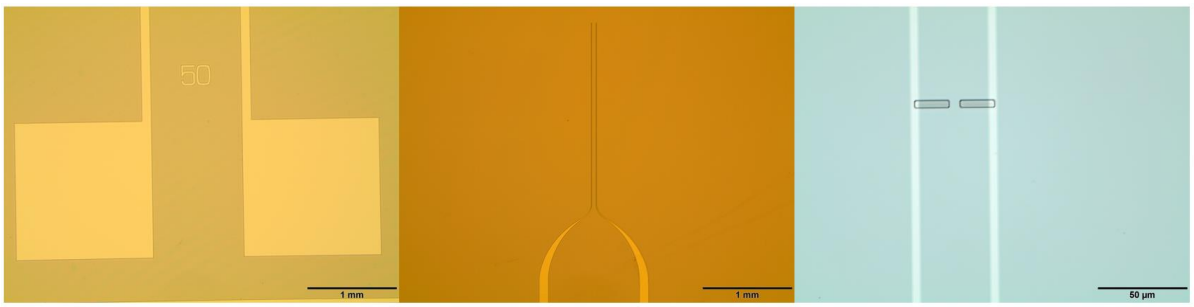
In total, different metal antenna structures, as well graphene antenna have been fabricated and delivered to UoS for further characterization

- Pd metal antenna on high resistivity silicon (HR-Si) with resistivity of 5 kΩ·cm
- Au metal antenna on HR-Si (5 kΩ·cm)
- Pd metal antenna on GaAs
- Au metal antenna on GaAs
- Pd metal antenna on Si+ ion implanted high resistivity silicon (HR-Si+) with resistivity of 5 kΩ·cm
- Pd contacted graphene antenna on HR-Si+ (5 kΩ·cm)

The characterization of the antennas will be discussed in Section 3. Below in Figure 8 are the micrographs of the metal antenna and graphene antenna.



(a)



(b)

Figure 8. Micrographs for (a) Pd metal antenna on implanted Si substrate, and (b) graphene antenna with Pd bottom contact on implanted Si substrate.

3 Characterization of Graphene Antenna

Terahertz time-domain spectroscopy (THz-TDS) was used to measure the THz field emission from the graphene dipole antenna. The dipole antenna was excited optically in its gap by a femtosecond laser pulse, which generates photocarriers in the semiconductor area that are accelerated from one antenna arm to the other due to an applied bias. This movement of charges leads to an emission of a picosecond pulse (THz frequency range) that is detected [Burford2017], in the case of the measurements performed in this work, by another photoconductive antenna. The spectrum obtained in this technique is the amplitude of the emitted signal in the time-domain. The emission signal in the frequency-domain can be calculated by means of Fourier transform.

3.1 Metal Antennas Measurement

Different antenna configurations were measured in order to evaluate the impact of each material change from a traditional Au antenna on GaAs to a graphene antenna on silicon substrate.

3.1.1 Antennas on HR-Si Substrate

Four different antenna configurations (Au/GaAs, Pd/GaAs, Au/HR-Si and Pd/HR-Si) with the same antenna design and material thicknesses were manufactured by AMO and measured by UoS.

It is possible to observe by Figure 9 that the change of metal has a very small impact in the emitted signal, while the change of substrate from GaAs to HR-Si was the main reason of the decrease of the emitted signal, which was not even possible to be measured at 10 mW of excitation.

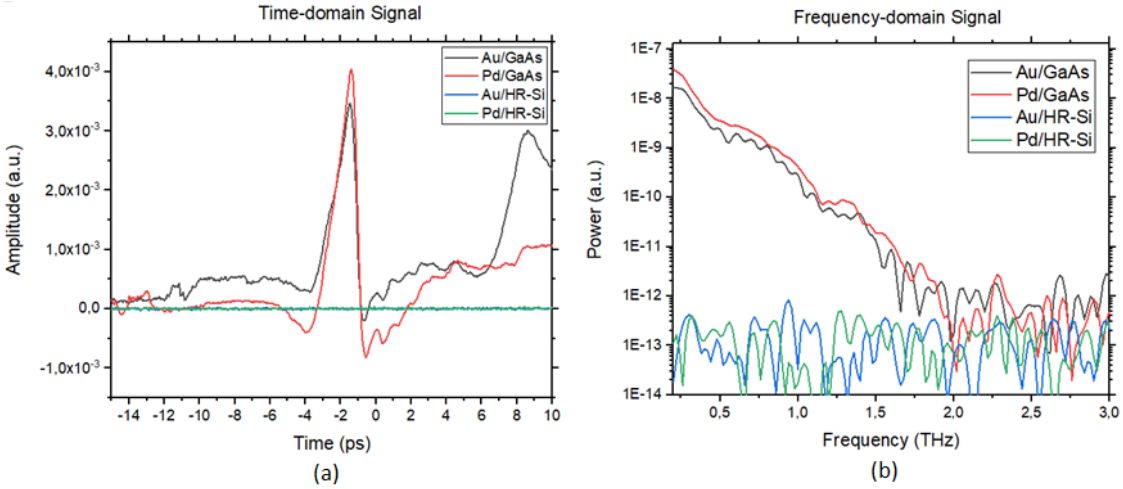


Figure 9. Comparison between the different antenna configurations at 10 mW and 10 V, (a) time-domain and (b) frequency-domain.

The antennas on HR-Si show a typical behavior of increased emission by increased applied bias, as can be seen in Figure 10a.

Further analysis was done regarding the almost zero emission of the antennas on HR-Si substrates and it was found that this kind of antenna configuration suffers from a

very strong field screening. By using high excitation powers, the carriers accumulate and this makes the electric field present on the antenna arms to decrease, leading to a lower emission. The screening effect can be observed in Figure 10b, where the emission of an Au/HR-Si antenna was measured by keeping the applied bias constant and varying the excitation power.

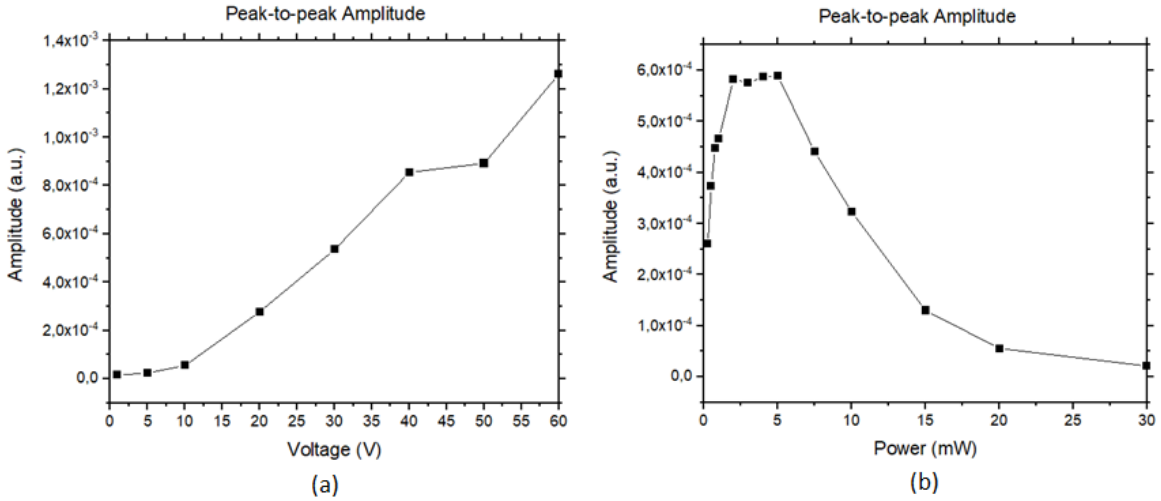


Figure 10. Amplitude emission of an Au/HR-Si antenna by (a) keeping a constant bias of 30 V and varying excitation power and (b) keeping an excitation power of 5 mW and varying the applied bias.

After around 5 mW of excitation power, the metal antennas on HR-Si starts to present a lowering of the emission until a point it gets to the same level of the noise signal.

For an effective emission comparison between the antennas on GaAs and on HR-Si, a low excitation power was used. In Figure 11, it is possible to observe the decrease of around 20 dB emission in power by only changing the material substrate.

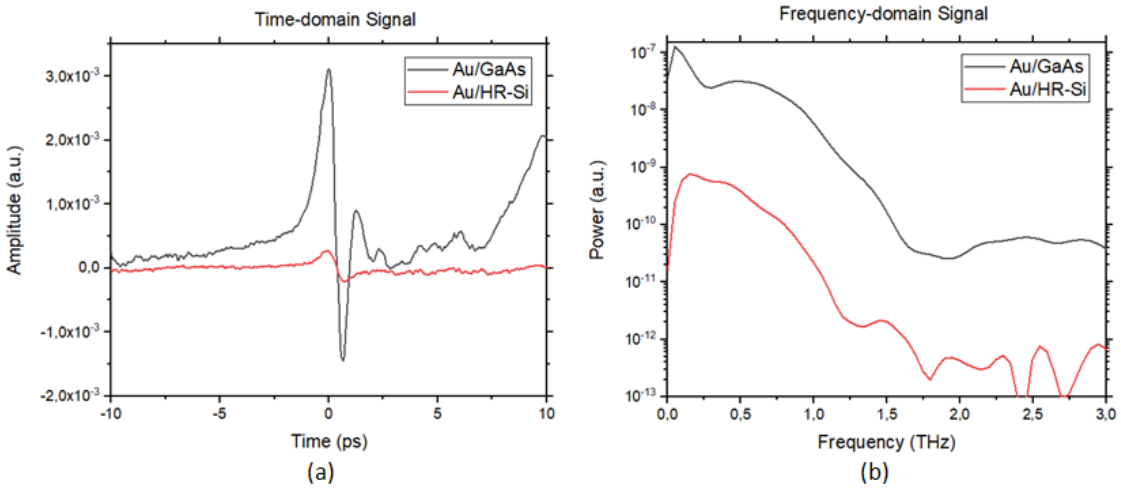


Figure 11. Emission comparison between an Au/GaAs and an Au/HR-Si antenna at 1 mW and 30 V in (a) time-domain and in (b) frequency-domain.

It was possible to measure an emission of an metal antenna on the HR-Si with low excitation power.

3.1.2 Antennas on HR-Si+ Substrate

To overcome the field screening issue and be able to use high excitation powers, Si+ ion implantation was done in the HR-Si substrate to create defect sites where e-h could recombine reducing the accumulation of charges in the antenna arms. As in the previous section, metal antennas were firstly measured in order to have a fair comparison to the graphene antennas in therms of emission efficiency from.

From Figure 12, it is also possible to observe the big impact of the change of substrate. The use of a HR-Si+ substrate instead of a GaAs, presents a decrease of emission around 20 dB in power. Nevertheless, it was still possible to measure the emission at 10 mW, what was not possible before due to the huge decrease of emission from 5 mW using the HR-Si substrate.

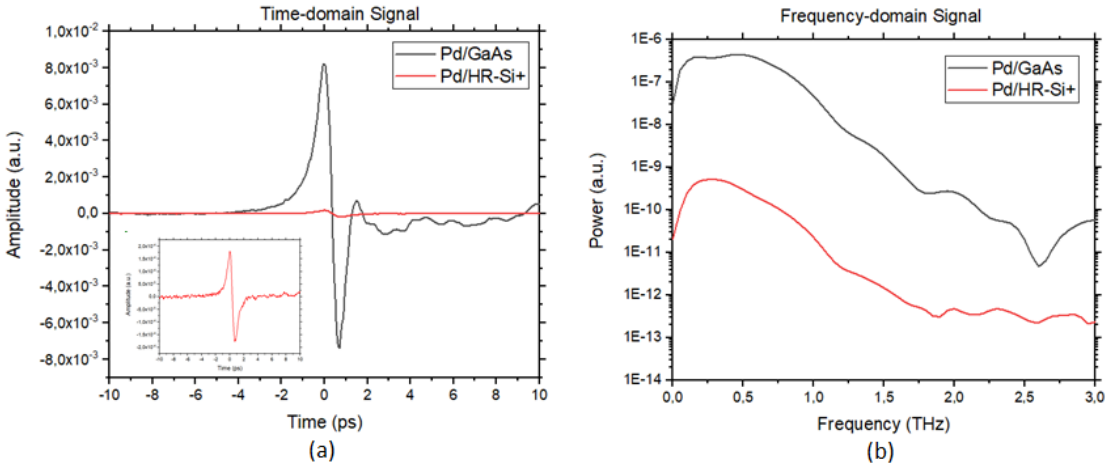


Figure 12. Emission comparison between a Pd antenna on GaAs and a Pd antenna on HR-Si+ at 10 mW and 30 V. (a) Time-domain measurement results, (b) Frequency-domain measurement results.

To evaluate the screening effect on this HR-Si+ substrate, different measurements with varying voltages and excitation powers were performed. In Figure 13, it is possible to observe that, the use of a HR-Si+ substrate instead of HR-Si reduces the screening significantly, allowing the use of high excitation powers to the antenna without the decrease of the emitted THz radiation.

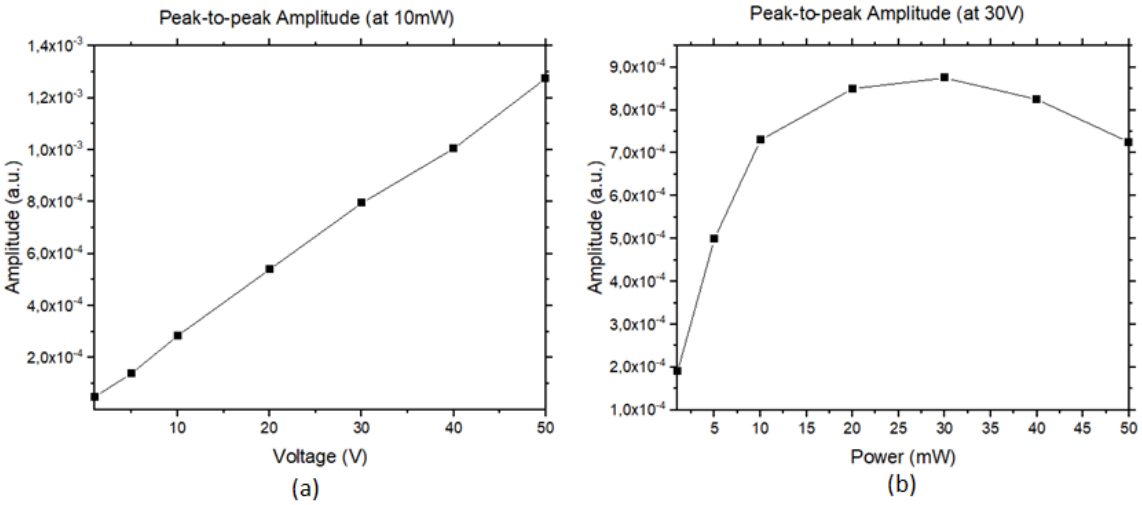


Figure 13. THz emission of a Pd antenna on HR-Si+, (a) with constant power and varying voltage and (b) with constant voltage and varying power

For the Pd antennas on HR-Si+, increased voltages lead to increased emission. Also, by using increased excitation powers the emission increases until saturation around 30 mW.

3.2 Graphene Antennas Measurement

With the issue of the screening solved by the use of the HR-Si+ substrate, graphene antennas on top of such substrates were fabricated by AMO and measured by UoS.

In Figure 14 one can see the comparison between a Pd antenna and a graphene antenna on the HR-Si+ substrate. There is a clear decrease in the emission of around 15 dB in power only by the change of the antenna material from Pd to graphene.

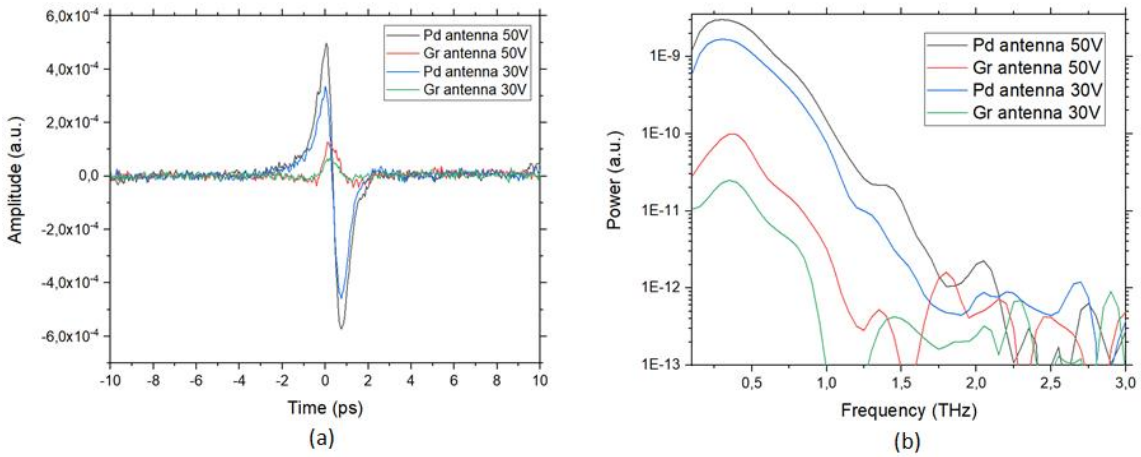


Figure 14. Comparison of a Pd/HR-Si+ antenna and a graphene/HR-Si+ antenna at 10mW and 30 and 50V in (a) time-domain and (b) frequency-domain

As the metal antennas, the graphene antenna also present an increase in emission with increasing applied bias (Figure 15a), differently than when one increases the excitation power. The graphene antennas start to present a strong screening after 0.5 mW, as can be seen in Figure 15b and c.

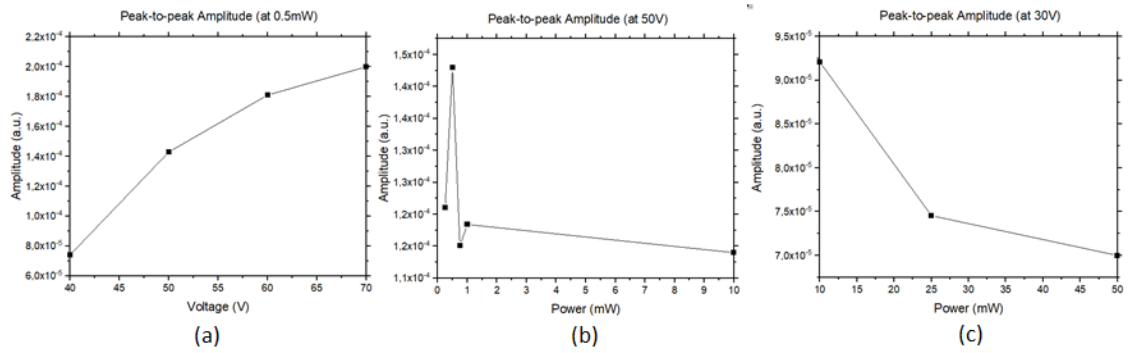


Figure 15. emission amplitude (a) by increasing the voltage at constant 0.5 mW, (b) varying the excitation power at constant voltage of 50 V and (c) varying the excitation power with constant voltage of 30 V

Even though with screening present in the graphene antenna on HR-Si+, it is still possible to see a clear THz emission of the samples analyzed. Figure 16 shows the result of a 1000 measurement of one of the samples.

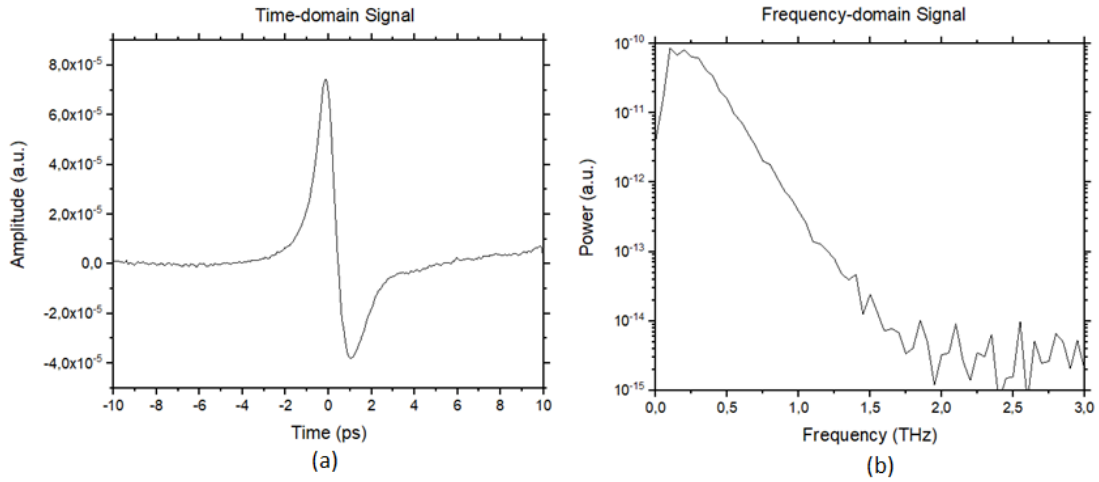


Figure 16. Average of 1000 measurements of a graphene antenna on HR-Si+ at 0.4 mW and 60 V in (a) time-domain and (b) frequency-domain.

These results confirm the possible use of graphene antennas on top of silicon substrates for SiGe technology integration.

4 Through Substrate Via

Through substrate via is significant for realizing co-integration of graphene antenna with SiGe technology, as well as other technology platform. Here we will first introduce the through substrate via process on PI, and then the through glass via.

4.1 Through Substrate Via on Polyimide

A process was developed to create the electrical connection between the top metal and the bottom ground metal, as shown in the red dashed box of Figure 17. However, to make the microprocesses possible, one needs Si as supporting substrate during the process. As one can see from the illustration, another PI layer between the Si and the bottom ground metal is necessary to make the delamination of the flexible part off the Si substrate possible after all the fabrication steps finish. This process is useful for monolithic microwave integrated circuit (MMIC) process, but there is a limitation for the use in the co-integration of graphene antenna, because on one hand the thickness of the PI (8 µm) is too small for our targeted wavelength. On the other hand, the additional bottom PI layer is necessary to realize the delimination, which makes the bonding to target wafer with electrical connection not easy.

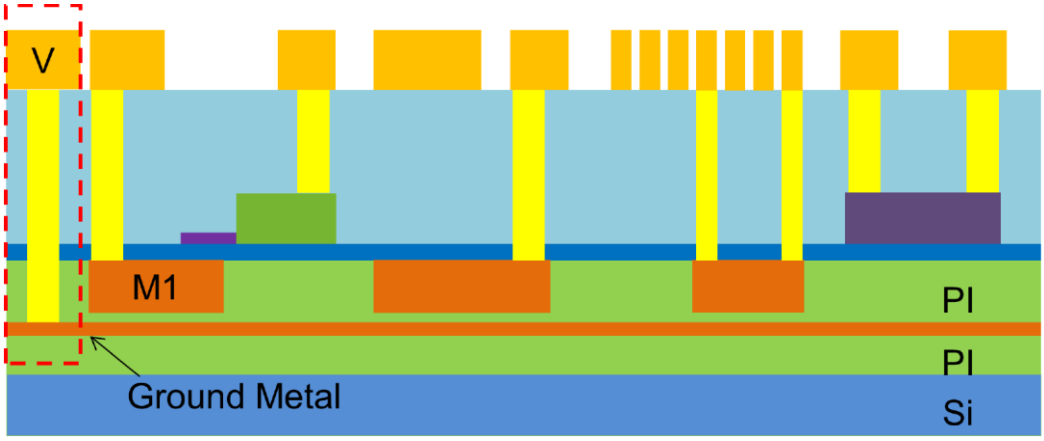


Figure 17. The through substrate via on the top PI layer.

4.2 Through Glass Via

Through glass via (TGV) fabrication is provided as a service at the company SCHOTT. Since TGV is not possible to be fabricated with the available tool at AMO, it is decided to purchase wafer with TGV from SCHOTT. This kind of glass wafer will be delivered with predefined via hole through the substrate, which enables the electrical connection between the front and back side of the wafer. Afterwards the graphene antenna will be fabricated on the front side and connected to the targeted underlying circuits. A illustration of such vias is shown in Figure 18.

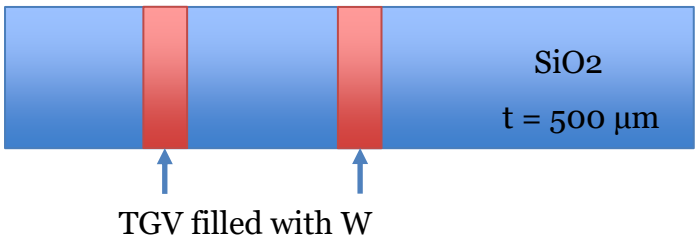


Figure 18. TGVs which are filled with metal W (tungsten).

The properties of such a glass substrate is summarized in Table 1. The electrical properties have been confirmed by RWTH with simulation, and the fabrication of TGV will be carried out on such a substrate.

Table 1. Physical Property of SCHOTT D 263® T eco

SCHOTT D 263® T eco

Glass type	Borosilicate
CTE α (20 °C; 300 °C) in 10^{-6} K^{-1}	7.2
Transformation temperature T_g in °C	557
Density p in g/cm³	2.51
Young's modulus E in GPa	72.9
Refractive index (as drawn) n_D	1.5230

	λ in nm	τ in %	τ_i in %
UV transmission at a thickness of 1 mm[8)]	308	0.2	0.2
	355	87.4	96.1

Frequency in GHz[3)4)]	**1**	**2**	**5**	**24**	**77**
Dielectric constant (permittivity) ε_r[2)]	6.4	6.4	6.3	6.3	6.1
Loss tangent $tan(\delta)$ in 10^{-4}	74	81	101	210	240

Specific electrical volume resistivity ρ_D at 50 Hz	ρ_D at ϑ = 250 °C in Ω·cm	$1.6 \cdot 10^8$
	ρ_D at ϑ = 350 °C in Ω·cm	$3.5 \cdot 10^6$

5 Design of SiGe Chip

An integrated circuit (IC) chip is submitted for fabrication using the IHP SG13G2 technology with f_t/f_{max} = 300/500 GHz, 7M/MIM. The submitted design occupies less than 2.9 mm^2 chip area as shown in Figure 19. The following sections discuss each component in the top-level layout. This activities and resources incurred by the partners UoS (Tx/Rx reference design, fabrication and test) and RWTH (transceiver design for graphene antenna integration) are supportive activities to the project. Two MPW SiGe chip-runs have been provided to the project as additional contributions beyond the project, in order to enable this remarkable success.

The submitted design combines standalone millimeter-wave transceiver building blocks to evaluate the performance limitations and possible scaling of the transceiver at higher frequencies exploring distinct approaches. After the fabrication and characterization of the circuits, they will be compared to the conventional implementations on the same technology or other relevant technologies.

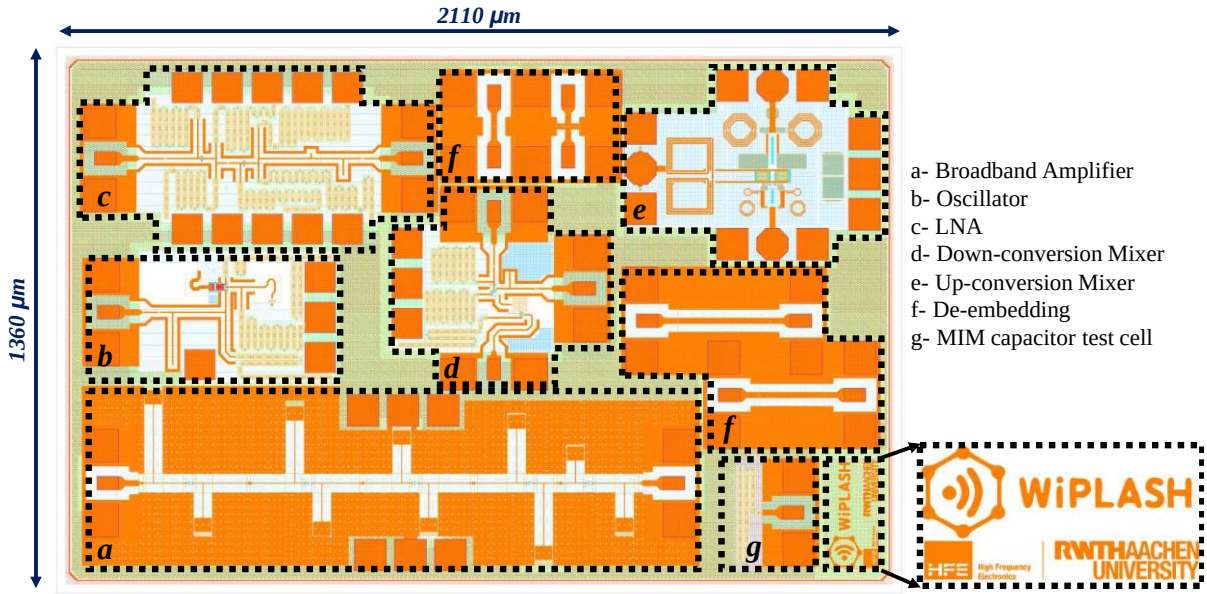


Figure 19. Layout of the submitted design occupying 1.36 mm x 2.11 mm.

5.1 Broadband Amplifier

The block labeled (a) in Figure 19 is a five-stage common-emitter broadband amplifier. The amplifier is designed to provide a bandwidth of 120 GHz centered at 180 GHz. The simulated gain ranges between 14.5 dB - 16.7 dB, the linearity (P_{1dB}) is > -10 dBm, and the power consumption is 16.5 mW. The chip area of the amplifier is 440 µm x 1250 µm. The layout of the amplifier is presented in Figure 20.

Figure 20. Layout of the broadband amplifier occupying 0.55mm^2.

5.2 Oscillator

The block labeled (b) in Figure 19 represents a Colpitts oscillator. The simulated oscillation frequency is 150 GHz with a phase noise of -102.4 dBc/Hz at 10 MHz offset frequency. The output power of the oscillator is -11.4 dBm consuming 6.8 mW. The chip area of the oscillator is 330 μm x 640 μm. The layout of the oscillator is shown in Figure 21.

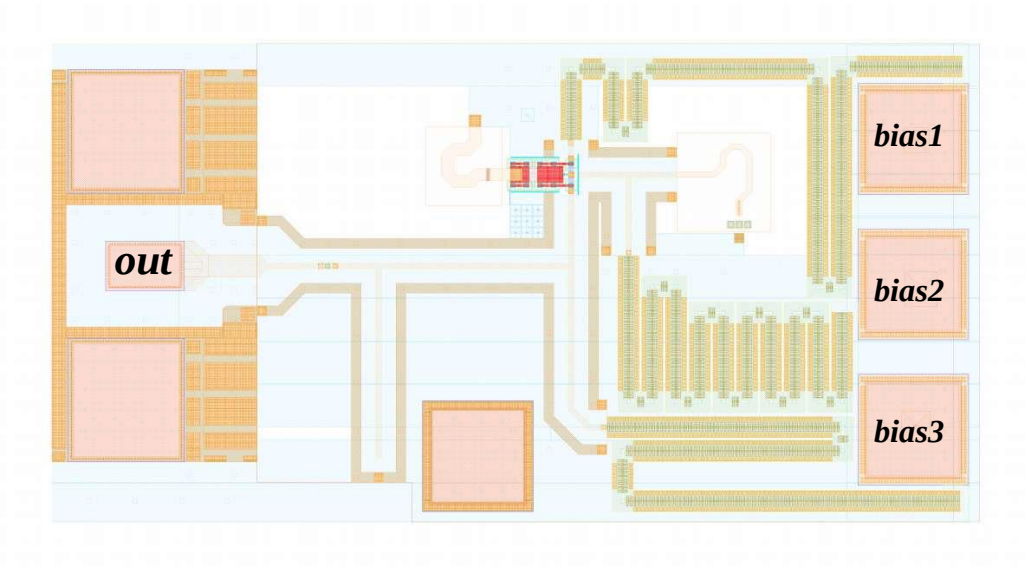


Figure 21. Layout of the Colpitts oscillator occupying 0.21mm^2.

5.3 Low Noise Amplifier

The block labeled (c) in Figure 19 represents a 2-stage cascade low noise amplifier (LNA). The simulated gain is 11.5 dB to 14 dB with a noise figure of 11 dB. Bandwidth of the amplifier is from 200 GHz to 240 GHz consuming 12.8 mW. The chip area of the LNA is 450 μm x 900 μm. The layout of the LNA is presented in Figure 22.

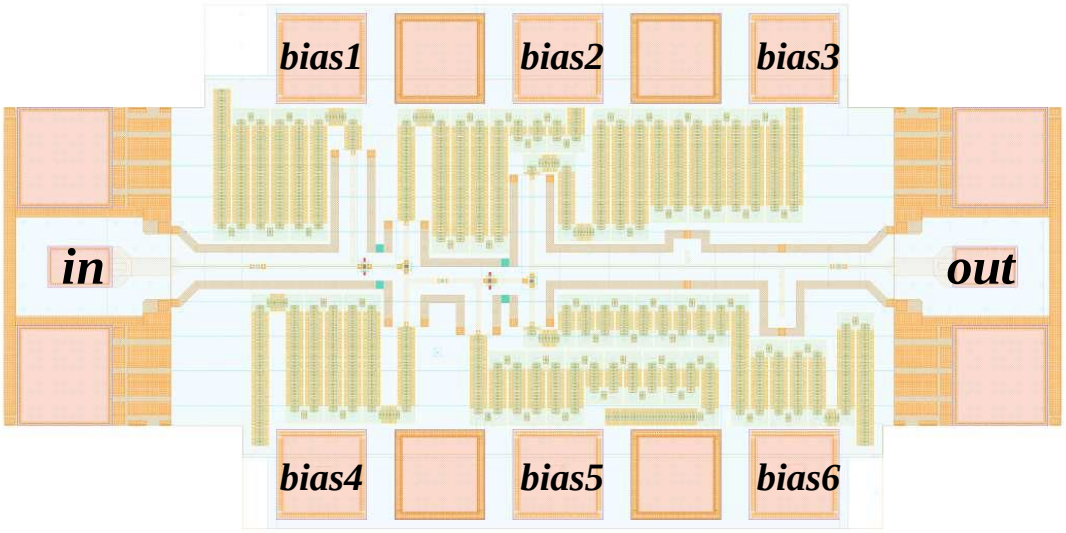


Figure 22. Layout of the cascode LNA occupying 0.405mm^2.

5.4 Active downconversion mixer

The block labeled (d) in Figure 19 represents an active downconversion mixer. The radio frequency (RF) frequency ranges from 200 GHz - 240 GHz while the local oscillator (LO) frequency ranges from 190 GHz - 230 GHz. The simulated conversion gain is 7.5 dB consuming 2.5 mW for an LO power of -10 dBm. The double-side band (DSB) noise figure is 14 dB. The chip area of the mixer is 500 μm x 500 μm. The layout of the mixer is presented in Figure 23.

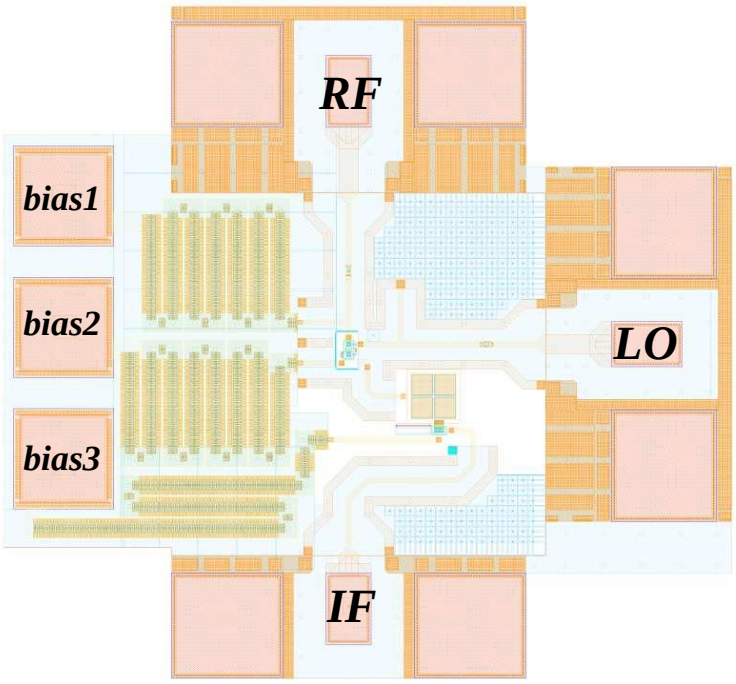


Figure 23. Layout of the active downconversion mixer occupying 0.25mm^2.

5.5 Subharmonic passive up-conversion mixer

The block labeled (e) in Figure 19 represents a subharmonic passive balanced up-conversion mixer. The mixer up-converts an intermediate frequency (IF) signal to RF output centered at 60 GHz using a LO signal at 30 GHz and LO power of 10 dBm. The simulated conversion loss is 6 dB providing more than 20 dB second harmonic suppression. The chip area of the mixer is 640 μm x 475 μm. The layout of the mixer is presented in Figure 24.

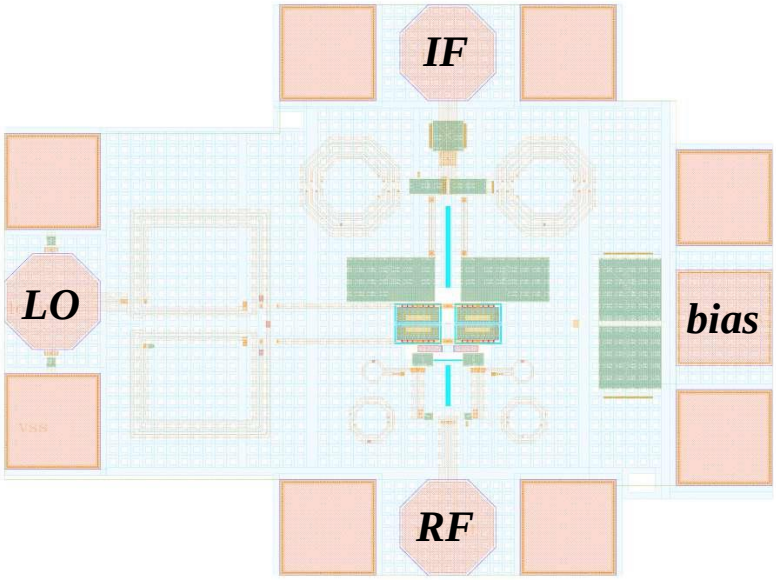


Figure 24. Layout of the subharmonic upconversion mixer occupying 0.3mm^2.

5.6 De-embedding and test structures

The blocks labeled (f) and (g) in Figure 19 represent de-embedding structures and metal-insulator-metal (MIM) capacitor test cell, respectively. The used de-embedding method in the standard short-open-load-through (SOLT) for on wafer measurements.

6 Integration

With all the elements decribed in previous sections, we are capable of realizing the co-integration of the graphene antenna to SiGe based transceiver.

Figure 25 presents a sketch of the target system. At the top level graphene antenna can be fabricated based on a scalable process developed at AMO. The antenna is electrically connected to the back side of the glass substrate by TGV. At the bottom it is the customized SiGe circuits.

Special consideration needs to be given on the dimension of all the building blocks, in order to make the integrated system compatible with desired frequency.

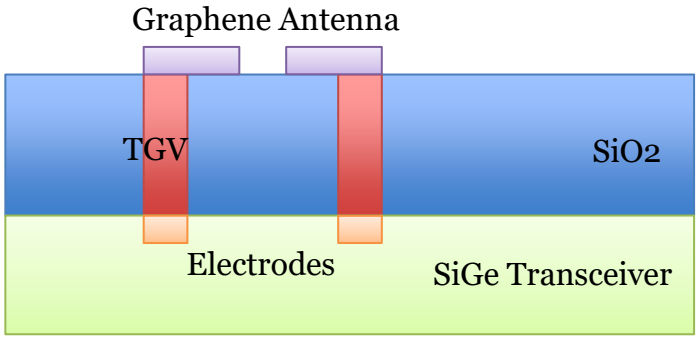


Figure 25. Co-integartion of graphene antenna and SiGe transceiver.

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