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Architecting More than Moore – Wireless Plasticity for Massive Heterogeneous Computer Architectures †

D1.1: SiGe BiCMOS test devices

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Legal Disclaimer

Executive Summary

This deliverable is the first report from WP1 RF Design and Implementation, which aims to develop reference test device structures to perform transmission channel measurements in the frequency range of 60-312 GHz. In order to integrate the antenna working in the terahertz range, a compatible transmitter and receiver design needs to be addressed. These test devices are of extreme importance to validate the performance of graphene antennae.

In the original proposal, one series of devices was planned. Given the very interesting results of the first chip run with extraordinary bandwidth, two generations of devices were developed. In this deliverable, the structure and measurements of a first generation of complete transmitter Tx and receiver Rx test devices for operation at 240 GHz are described with a bandwidth of 40 GHz fully integrated in a Silicon-Germanium (SiGe) foundry process alongside with bow-tie antennae. The measurement results are presented and discussed. The devices were manufactured as a foundry process via Europractice at the Leibniz Institute for High Performance Microelectronics (IHP), Frankfurt Oder, Germany.

The University of Siegen (UoS) performed a substantial experimental analysis and was able to demonstrate the operation of the SiGe transmitter and receiver chips. The output power of the transmitter chips and the internal local oscillator power levels of the receiver chips exhibited a very interesting bandwidth of 44GHz. The power level in the band center was 6dB lower and 4dB lower, when measured with circuits with and without antenna, respectively, compared to simulation.

A second chip run was put in place to take full benefit from the high bandwidth of the devices. Furthermore, to expand the operating band to 120 GHz, we have developed customized SiGe circuits operating at different frequencies in the THz range. All the required building blocks for a functional SiGe transmitter/receiver - amplifiers, mixers, ring oscillators, and so on - are discussed in details and simulations are provided. An initial prototype tape-out was submitted in Q1 2021 and the samples are expected to be characterized by the end of Q3 2021. The tape-out for the full T_x/R_x chips is predicted to be Q4 2021, as the foundry process was delayed due to the Corona pandemic. This is however not critical to the project, as a functioning first generation of chips is already available to the project, as originally planned.

Abbreviations and Acronyms

BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog
f_{max}	Maximum frequency of oscillation
f_T	Cut-off frequency
HWG	Hollow waveguide
IF	Intermediate-frequency
IHP	Leibniz Institute for High Performance Microelectronics
LNA	Low Noise Amplifier
LO	Local-oscillator
LPF	Low-Pass-Filter
MIM	metal-insulator-metal
NF	Noise Figure
PA	Power Amplifier
PCB	Printed Circuit Board
PN	Phase noise
Q3	Third Quarter
RF	Radio-Frequency
Rx	Receiver
SiGe	Silicon-Germanium
TRx	Transceiver
Tx	Transmitter
VGA	Variable Gain Amplifier

The *WiPLASH* consortium is composed by:

UPC	Coordinator	Spain
IBM	Beneficiary	Switzerland
UNIBO	Beneficiary	Italy
EPFL	Beneficiary	Switzerland
AMO	Beneficiary	Germany
UoS	Beneficiary	Germany
RWTH	Beneficiary	Germany

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1 Introduction

With the advance of communication technology in the past years due to the increased connectivity of digital devices, there was the need for even higher data-rate communication systems to be developed [1]. Unfortunately, the typical alternative to fulfill this purpose, *i.e.* using smaller components and more cores processors, reached its limit due to the increase of energy consumption related to wiring losses that start to play a significant role when billions of components are placed in one single chip [2].

The use of wireless links could enable the speed increase in inter/intrachip communication. For this, a large bandwidth is required, which could be solved by the use of higher center frequencies, *e.g.* submillimeter-wave (sub-mm-wave) range frequencies. The vision of the WiPLASH project of going further into wireless communication in the THz range could be achievable by the use of antennas working in this frequency range and compatible transmitter and receiver units.

The discovery of plasmons in graphene opened the path for designing and developing graphene antennas operating at THz frequencies, which could be smaller in size compared to the conventional metal antennas and also tunable by controlling some of the graphene material characteristics [3], [4]. Besides, transceiver devices working in the hundreds-GHz frequency could be developed due to the progress of the semiconductor technology process, delivering faster transistors in the Complementary Metal-Oxide-Semiconductor (CMOS) and SiGe Bipolar Complementary Metal-Oxide-Semiconductor (BiCMOS) technologies. Several transceivers with on-chip antennas working in the range of 100-300 GHz using different modulations were already demonstrated using these recent transistor technologies achieving high data rates [1], [5], [6], [7], [8], [9], [10]. Higher data transfer in wireless links is achievable by the usage of wider bandwidth. For this, a transmitter and a receiver with a wide operational frequency are essential to utilize the sub-mm-wave range [1].

The block diagram in figure 1 illustrates a simplified RF transmitter frontend.

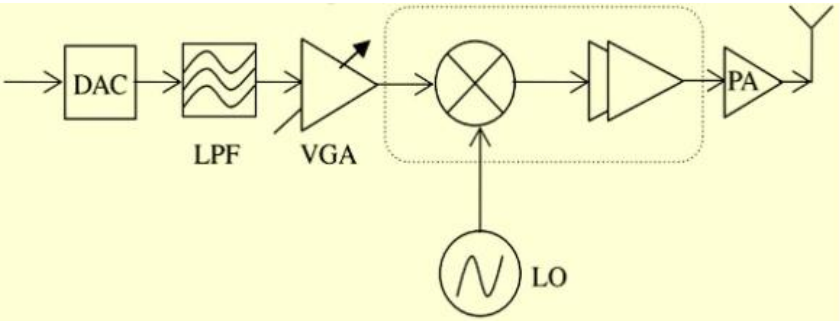


Figure 1: Block diagram of an RF transmitter frontend [11]

A standard transmitter frontend is based on a digital-to-analog converter (DAC), a low-pass filter (LPF), a variable gain amplifier (VGA), a local oscillator (LO), an up-conversion mixer, a transimpedance driver amplifier, and a power amplifier (PA). It generates a stable RF signal by combining the analog and the LO signals to an up-converted RF signal, which will be modulated in frequency, phase or amplitude. This modulated signal will be driven to the antenna with a PA [11], [12].

A simplified building block of an RF receiver frontend is shown in figure 2.

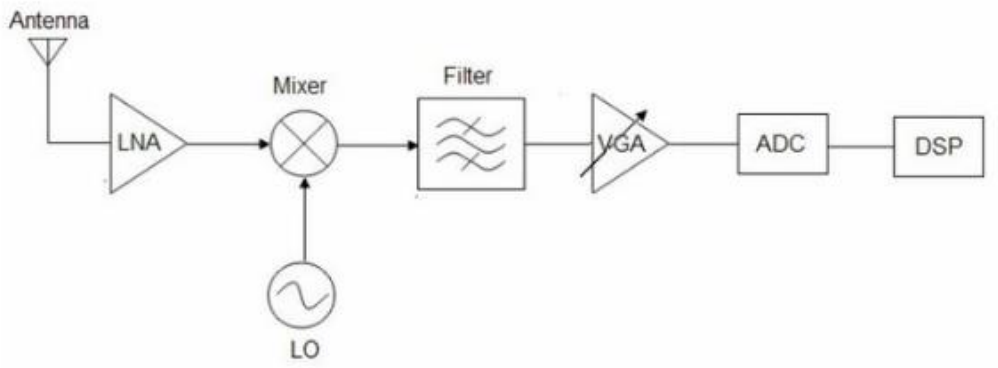


Figure 2: Block diagram of an RF receiver frontend [13]

A basic RF receiver frontend consists of an antenna, a low-noise amplifier, a mixer, a local-oscillator, a filter, and an analog-to-digital converter. It converts the RF signal received by the antenna and amplified by the low-noise amplifier to a lower intermediate frequency (IF) by mixing it with the signal from the local oscillator [12], [13].

This report is focused on the design and measurement results of a transmitter and a receiver frontend in the sub-mm-wave range using the SiGe BiCMOS SG13G2 technology. A transceiver and receiver with a bandwidth of 40 GHz and center frequency at 240 GHz with an on-chip antenna are presented and characterized and, for an increased operating band of 120 GHz, new circuits block designs and simulations for a future transmitter and receiver are shown.

2 Fully Integrated SiGe test devices at 240 GHz

Preliminary channel measurements were performed using transmitter and receiver SiGe test devices developed and fabricated by foundry process via Europractice at IHP Frankfurt Oder. This activity had the goal to demonstrate the good performance of transceiver and receiver devices integrated with antennas at THz frequency range, namely 220-260 GHz.

2.1 Design

The transmitters and receivers used were devices from the SG13G2 technology. The SG13G2 is a 0.13 µm BiCMOS technology with a cutoff frequency of 300 GHz and a maximum frequency of 500 GHz [14].

The design of the transceiver and receiver chips are shown in figure 3. Figure 3-a, c show the block diagram of the SiGe chips and figure 1-b, d show the microscope pictures of the finished components.

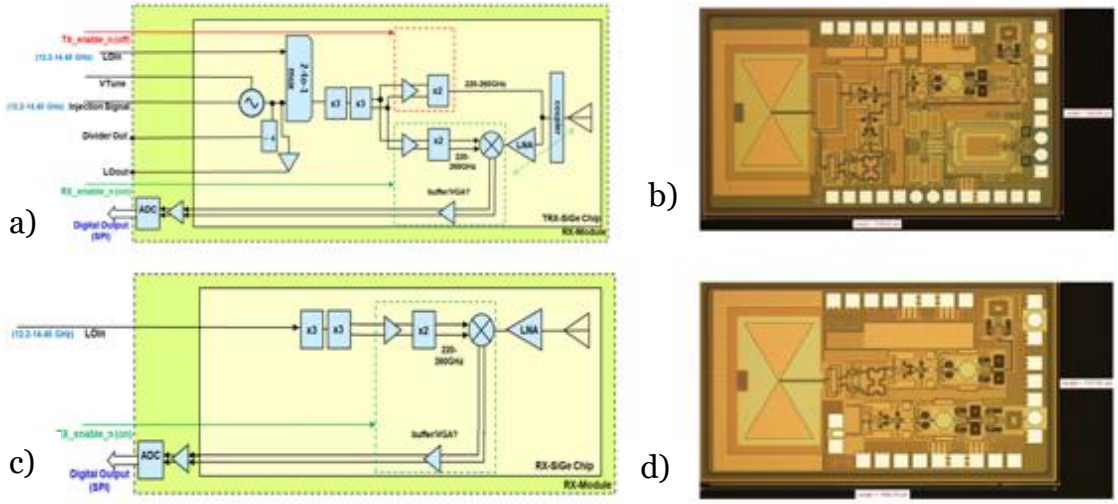


Figure 3. SiGe chips, a) block diagram of the TRx chip, b) microscope image of the TRx chip, c) block diagram of the Rx chip and d) microscope image of the Rx chip.

The transceiver component consists of a chip with an area of 2136.55 x 1249.64 µm² and the receiver component of an area of 1890.76 µm x 1127.83 µm. Both chips are fully integrated with a bow-tie antenna.

2.2 Measurements

For characterization, the chips were first placed on circuit boards and wire bonded to supply the DC voltages and high-frequency signals required for operation. The chips on the boards were each provided with a silicon lens with a simulated gain of 25 dBi. The TRx chips were glued on the backside of the lens (figure 4). The Rx chips were also placed on printed circuit boards (PCBs) using a silicon lens and characterized.

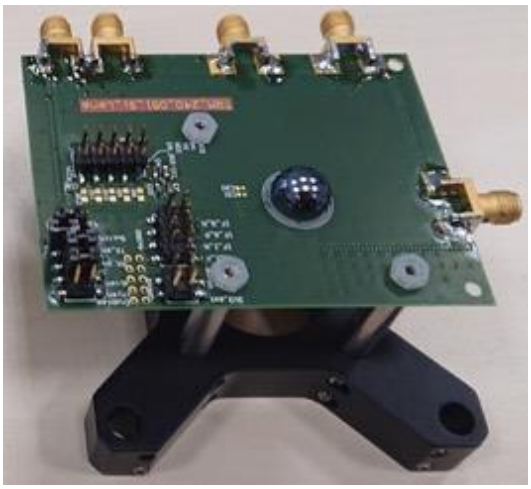


Figure 4: SiGe transceiver element with silicon lens and holder (cage plate)

The following measurements were performed for the characterization of the devices:

- Determination of the output spectrum of the transmitters, when operated via an external local oscillator signal at 22 frequencies between 220 GHz and 325 GHz for 9 input levels between -20 dBm and 6 dBm for each of 3 different supply voltages and 2 operating modes at room temperature
- Determination of the conversion gain of the receivers, when operated via an external local oscillator signal at 22 frequencies between 220 GHz and 325 GHz for 9 input power levels between -20 dBm and 6 dBm for each of 3 different supply voltages and 2 operating modes at room temperature and both differential outputs (I and Q), respectively, at an intermediate frequency of 1.8 MHz

2.2.1 Transmitter Characterization

In the characterization of the transmitter devices, a hollow waveguide mixer with a horn antenna of 24 dBi gain and known conversion losses was used. The characterization was performed in transmission at a distance between lens and horn antenna of 2.5 cm or distances in the far-field of 40 cm (figure 5).

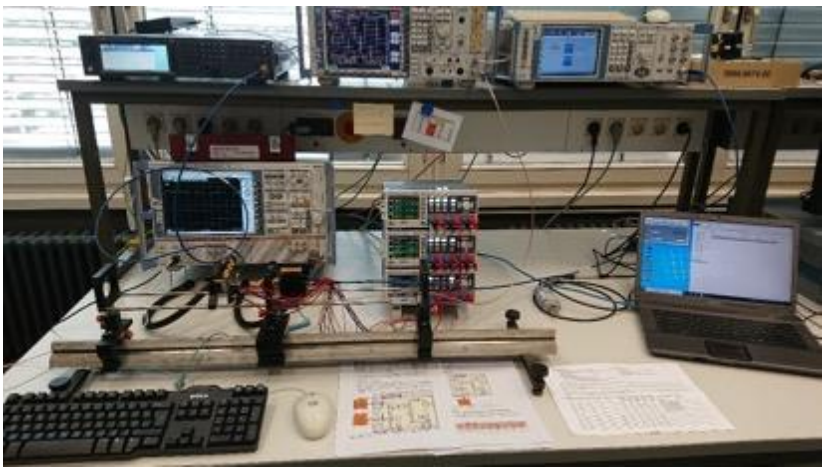


Figure 5: Characterization setup with all measurement devices. Under test, a SiGe transmitter and receiver with a hollow waveguide source

Figure 6 shows the radiated power of a SiGe transmitter with a silicon lens at different local oscillator (LO) power levels of the input signal. Due to the known distance between transmitter and receiver and, thus, the known free space attenuation, the known gains of lens and antenna, as well as the conversion losses of the receiver, the absolute power of the SiGe transmitter, as shown, could be determined via the Friis equation. The signals, which drop to lower frequencies, can be explained by the typical receiving characteristics of the hollow waveguide mixer used for characterization. A stable output signal with a bandwidth greater than 40 GHz was measured at LO input power levels above -12 dBm.

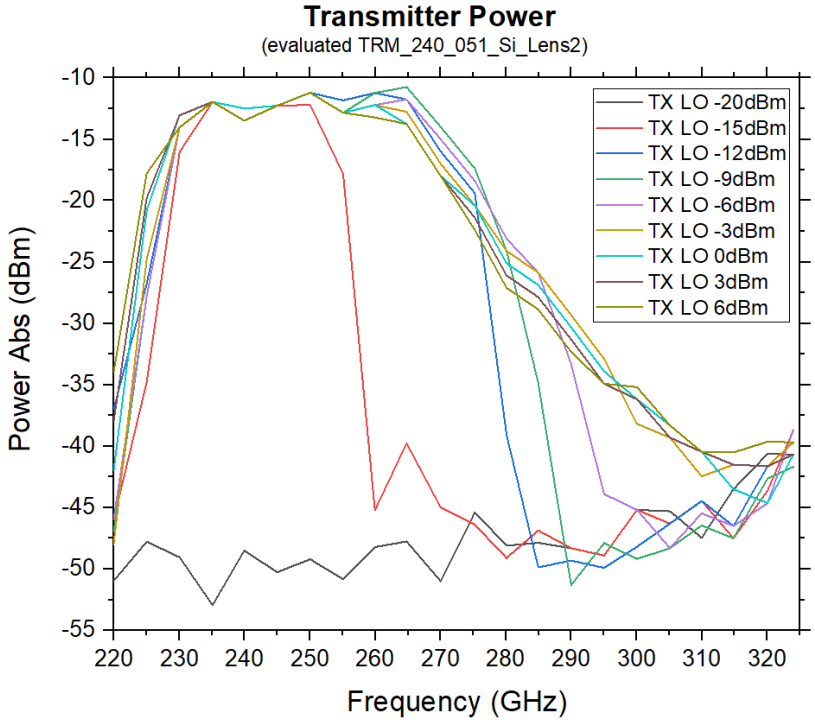


Figure 6: Radiated power of a SiGe transmitter at varying LO input power levels from -20 dBm to 6 dBm

Comparing the curve for the measured power (continuous curve) and the simulated power (dashed curve) in figure 7 between 230 GHz and 270 GHz, the power levels deviate between 5-6 dB. This flattening is also visible in measured curves plotted in figure 7. The reason was identified in the transmitter circuit and corrected for the 2nd design already taped-out and received by UoS for starting characterization on Septembert 2021.

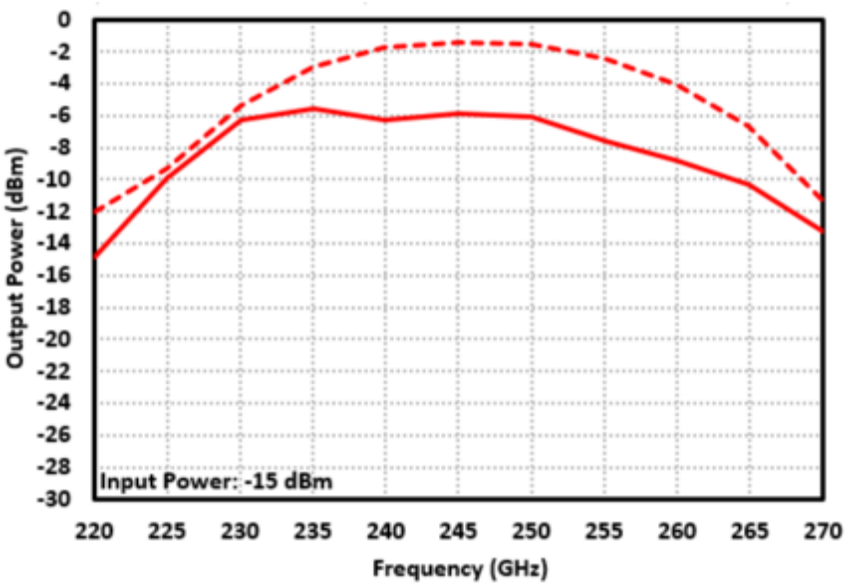


Figure 7: Probe station measured power (red curve) and simulated power (dashed curve) at the output of the multiplier chain at a LO input power of -15 dBm

2.2.2 Receiver Characterization

In the characterization of the receiver elements, a hollow waveguide source was used with a horn antenna with a gain of 24 dBi and known emission spectrum. The characterization was performed in transmission at a distance between lens and horn antenna of 2.5 cm or distances in the far field of 40 cm.

Figure 8 shows the conversion losses of a SiGe receiver with a silicon lens. Due to the known distance between the transmitter and receiver and, thus, the known free space attenuation, the known gains of the lens and antenna, and the known emission spectrum of the transmitter, the conversion gain of the SiGe receiver could be determined via the Friis equation. It should be noted here that the distance between the transmitter and receiver was smaller compared to the characterization of the SiGe transmitter and it was not in the far-field, as required by the Friis equation. This leads to deviations between measured power levels and power levels determined using the Friis equation, but this turned out to be a minor issue, as it will be shown in the following characterization in figure 9. Figure 8 shows that high-frequency signals with a bandwidth of at least 40 GHz can be converted to the intermediate frequency range from LO input power levels at the receiver of -15 dBm and above. Again, as in the characterization of the SiGe transmitter before, the curve of the conversion losses between 230 and 270 GHz at input power levels greater than -15 dBm shows a slightly reduced power. This was also corrected in the 2nd chip design already taped-out and receiver by UoS for starting characterization on September 2021.

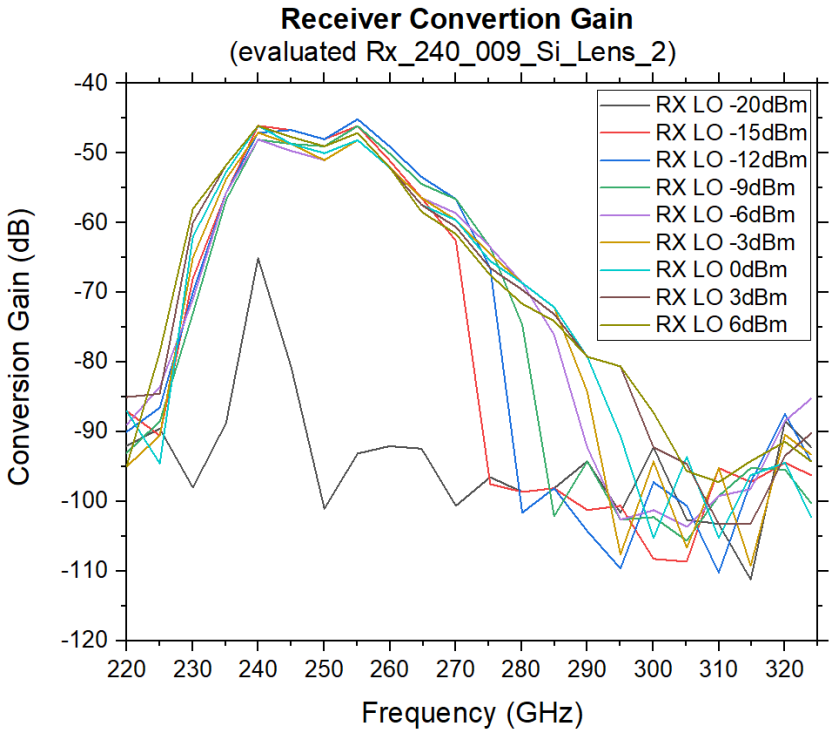


Figure 8: Conversion gain of a SiGe receiver at varying LO input powers from -20 dBm to 6 dBm

In addition to characterizing the individual SiGe transmitters and SiGe receivers, they were also operated and characterized together and compared to the individual measured spectra.

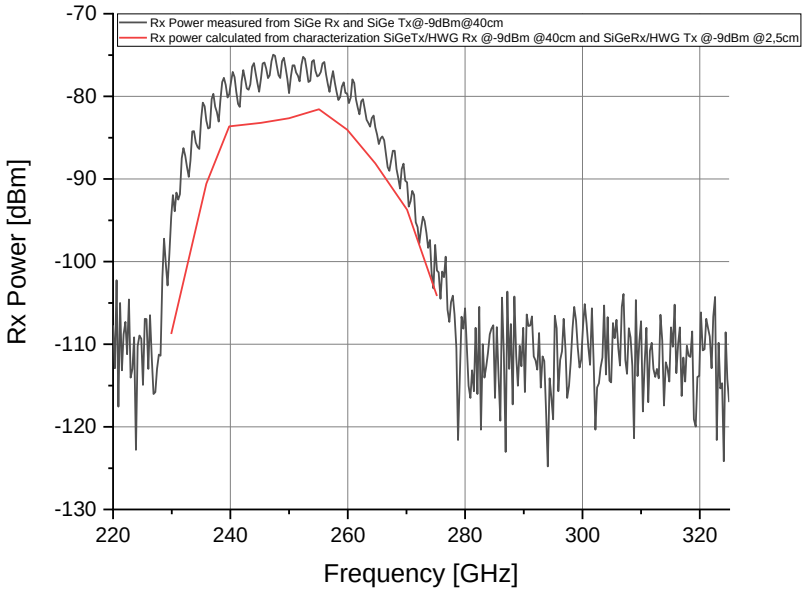


Figure 9: Comparison of the measured spectrum of the SiGe Tx and Rx (black curve) to the calculated spectrum from the SiGe Tx and hollow waveguide (HWG) Rx measurement and SiGe Rx and HWG Tx measurement (red curve)

The black curve in Figure 9 shows the measured spectrum from the previously characterized SiGe transmitter and receiver with silicon lens, that was set up at 40 cm distance in transmission. Both the transmitter and the receiver were operated with an LO input power level of -9 dBm. One can see an usable bandwidth of 44 GHz - which is 10% higher than the expected and simulated bandwidth of 40 GHz - and a dynamic range of about 30 dB. The comparison with the calculated spectrum from the independent measurements of the SiGe transmitter and receiver, previously characterized individually using a hollow waveguide (HWG) receiver, and the SiGe receiver (see Figure 7 red curve) shows, previously characterized with a HWG transmitter, good agreement and, thus, confirms all measured and calculated levels.

3 Dedicated SiGe Tx/Rx test device

A dedicated design to fulfill the requirements of modeling and system-level investigations is designed by RWTH and sponsored by UoS. The distinct integrated circuit consists of the Tx/Rx building blocks such as broadband amplifier, low noise amplifier, up-conversion mixer, down-conversion mixer, de-embedding structures, and oscillator. The tape-out is done utilizing the SiGe 0.13μm technology (SG13G2). The submitted design is under fabrication and the samples are expected to arrive for characterization by the end of Q3 2021. The chip occupies 1.36 mm x 2.11 mm including all probing pads and seal rings as described in figure 10. This chip design was already shown as part of the deliverable "D2.1: First co-integration of graphene antennas with full custom SiGe transceivers", but more details regarding simulation results of the building blocks are presented in the current report, as follows.

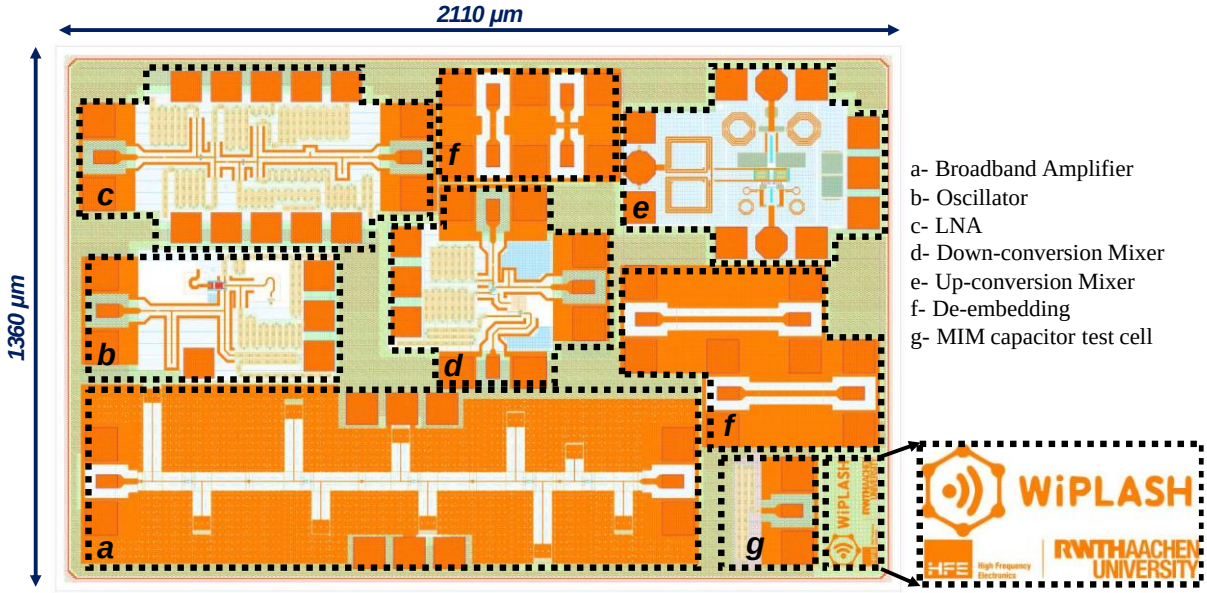


Figure 10. Layout of the submitted design occupying 1.36 mm x 2.11 mm of chip area.

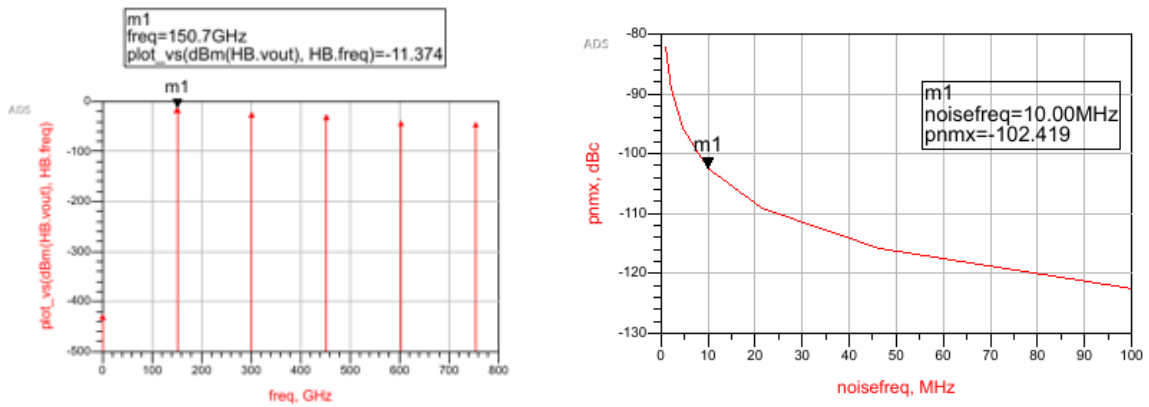
3.1 Broadband amplifier:

The broadband amplifier block labeled (a) in figure 10 is a five-stage common-emitter broadband amplifier. The amplifier is designed with a dedicated design procedure to provide a bandwidth of 120 GHz centered at 180 GHz. The simulated gain ranges between 14.5 dB-16.7 dB, the linearity (P_{1dB}) is > -10 dBm, and the power consumption is 16.5 mW. The chip area of the amplifier is 440 μm x 1250 μm. The layout of the amplifier is presented in figure 11.

Figure 11.Layout of the broadband amplifier occupying 0.55 mm^2.

3.2 150GHz low phase noise oscillator

The oscillator block labeled (b) in figure 10 represents a Colpitts oscillator. The simulated oscillation frequency is 150.7 GHz with a phase noise (PN) performance of -102.4 dBc/Hz at 10 MHz offset frequency as presented in figure 12. The output power of the oscillator is -11.4 dBm consuming 6.8 mW giving rise to the power efficiency of 1.1%. The chip area of the oscillator is 330 μm x 640 μm. The layout of the oscillator is represented in figure 13.



(a) (b)

Figure 12. Oscillator EM simulation results: (a) Output frequency and (b) PN.

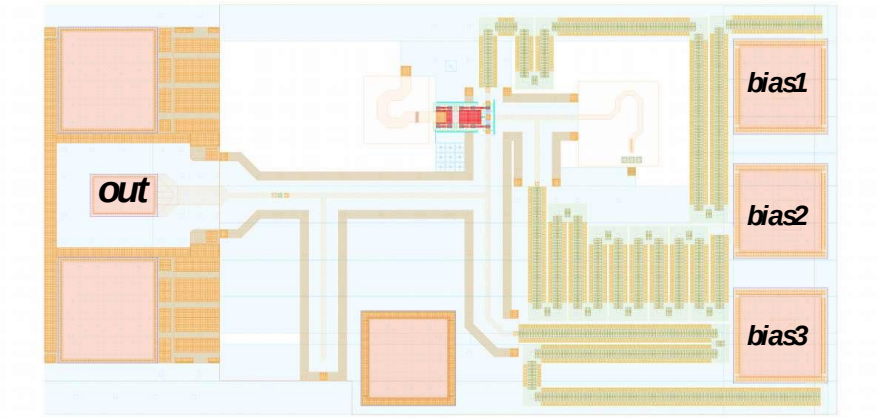
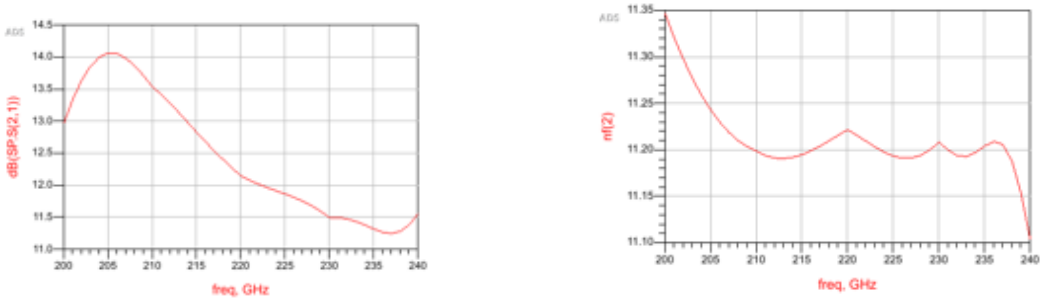


Figure 13.Layout of the Colpitts oscillator occupying 0.21 mm^2.

3.3 Low noise amplifier

The LNA block labeled (c) in figure 10 represents a 2-stage cascode design. The target frequency range is 200-240 GHz. Full EM simulations indicate a gain of 11.5 dB to 14 dB with a noise figure (NF) of 11 dB as shown in figure 14. The input 1-dB compression point is -25 dBm. The LNA consumes 12.8 mW and occupies a chip area of 450 μm x 900 μm including all DC and RF pads. The layout of the LNA is presented in figure 15.



(a) (b)

Figure 14. LNA EM simulation results: (a) Gain and (b) NF.

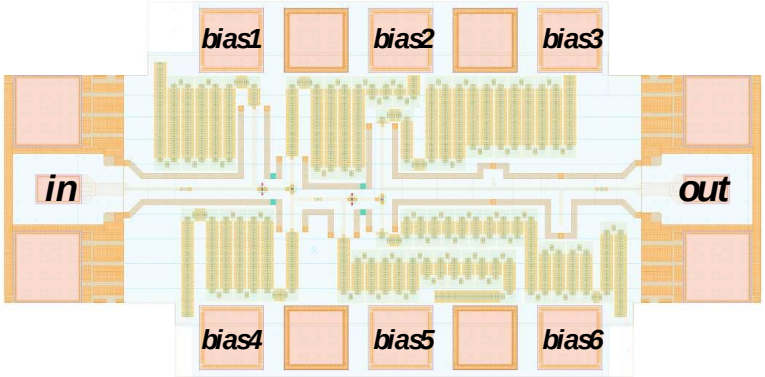


Figure 15.Layout of the cascode LNA occupying 0.405 mm^2.

3.4 200-240GHz 7.5dB conversion gain down-conversion mixer

The block labeled (d) in figure 10 represents an active down-conversion mixer. The radio frequency (RF) ranges from 200 GHz-240 GHz while the local oscillator (LO) frequency ranges from 190 GHz-230 GHz. The simulated conversion gain of the mixer ranges from 8.3 dB-7.2 dB with a DC power consumption of 2.5 mW and an LO drive power of -10 dBm as shown in figure 16. The double-sideband (DSB) noise figure is 14 dB. The chip area of the mixer is 500 μm x 500 μm. The layout of the mixer is presented in figure 17.

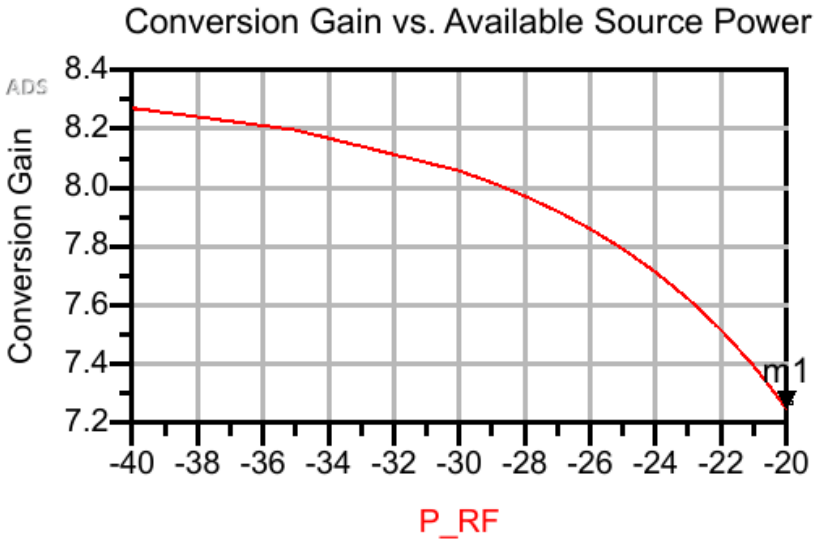


Figure 16. Simulated conversion gain of the active down-conversion mixer versus RF power.

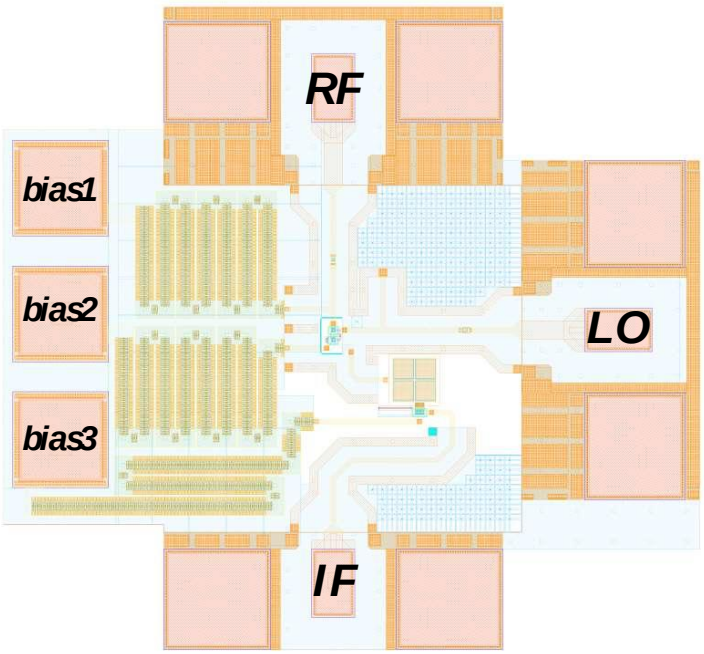


Figure 17.Layout of the active down-conversion mixer occupying 0.25 mm^2.

3.5 60GHz passive up-conversion mixer

The block labeled (e) in figure 10 represents a subharmonic passive balanced up-conversion mixer. The implemented design consists of a double-balance ring topology modified to include the bias voltage. Simulation results for the design show an up to 2 dB conversion gain for an IF varying from 100 MHz to 3.5 GHz. The 1 dB compression point occurs for an LO power of 12 dBm when the IF signal level equals -20 dBm and the bias voltage is set at -1 V, whereas it shifts up to 19.5 dBm for a -5 dBm IF signal level and a bias voltage of -1.5 V. Good isolation between LO and RF signals is achieved thanks to the designed baluns. For an LO of 13 dBm and an IF at 0.6 GHz and -10 dBm power, an isolation of 17 dB is achieved. The simulation results summary is represented in figure 18. The chip area of the mixer is 640 mm x 475 mm. The layout of the mixer is presented in figure 19.

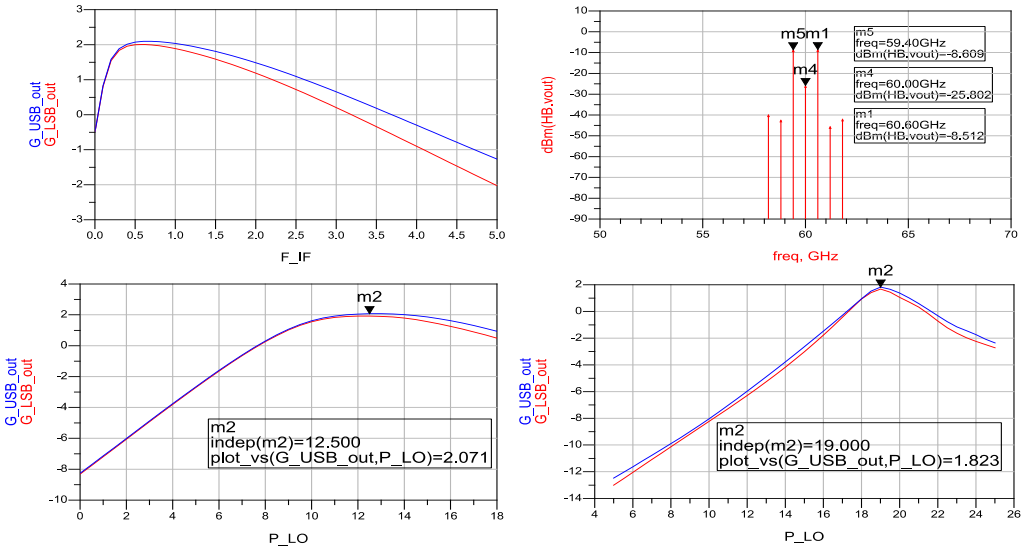


Figure 18.Simulation results of the designed subharmonic up-conversion mixer.

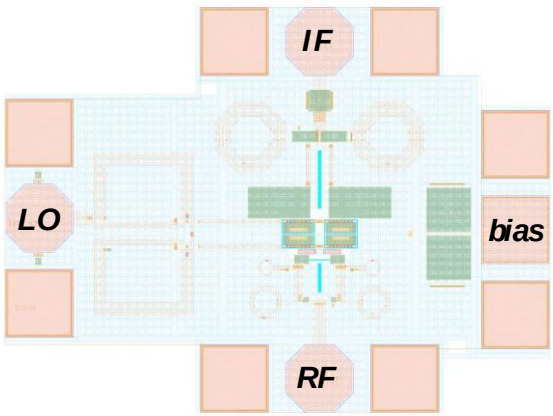


Figure 19.Layout of the subharmonic up-conversion mixer occupying 0.3 mm^2.

3.6 De-embedding structures and test cells

The blocks labeled (f) and (g) in figure 10 represent de-embedding structures and MIM capacitor test cells, respectively. The used de-embedding method is the standard short-open-load-through (SOLT) approach for on wafer measurements.

4 Summary of Results

The University of Siegen (UoS) greatly characterized the transmitter (Tx) and receiver (Rx) chips of the first Silicon Germanium (SiGe) wafer run at 220-260 GHz. Throught the results of these several measurements, the functionality of the transmitter and receiver chips were proved.

The target operation bandwidth was, in fact, increased by 10% from 40GHz to 44GHz. The output power level of the transmitter chips and of the internal local oscillatior (LO) of the receivers were measured as being 6dB and 4dB lower than simulated for the circuits with and without antennas, respectively.

Further area and power optimization options are investigated in a prototype designed by RWTH and sponsored by UoS to explore the possible implemenation of customised Tx/Rx chips. Two tape-outs are planned for this purpose. The employed technology is the SiGe 0.13 μm from IHP. The first tape-out consists of all building blocks and the tape-out was submitted in Q1 2021. The characterization of the fabricated chips is expected immediately after the arrival of the samples in Q3 2021. The second tape-out is planned to optimize the circuits according to the measurement results and exploit the optimized circuits the standalone building blocks and integrate them into the Tx/Rx systems.

In summary a first generation of fully functional Tx and Rx circuits was provided to the project, as originally defined in the project. An additionaly higher performance second generation of devices has been designed, fabricated, and is presently under analysis at UoS.

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